Heavy ion induce single event transient effects in SOI transistor

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ABSTRACT

With the scaling down of feature size, the proportion of region sensitive to single-event effect (SEE) with respect to active region increases. The simulation challenges the anti-radiation technology for space application. Silicon-on insulator (SOI) technology has been utilized for radiation hardened integrated circuits. This work takes advantages of TCAD tool to simulate SEE in SOI NMOSFET, focusing on the effects of linear energy transfer (LET) of injected heavy-ion, top silicon film thickness, drain bias, and floating body effect on single event transients (SET) pulse. Mechanisms are investigated, which provides guide for radiation hard SOI technology.

Keywords: Heavy ion, single event effect, parasitic effect, TCAD simulation

1. INTRODUCTION

With the increasing application of advanced semiconductor devices in military and aerospace fields, it is necessary to continuously enhance the reliability and lifetime of electronic systems. SOI technology shows good anti-SEU (single event upset) and anti-dose rate capabilities under space radiation conditions. Previous works show that the SET (single event transient) pulse widths are significantly shorter in SOI technologies than similar bulk technologies[1] which is very helpful for radiation-hardened device and circuit designs.

SOI MOSFET is more resistant to single event effects than ordinary bulk silicon MOSFET, mainly due to isolation oxide. The active region of bulk silicon MOSFET sits in the substrate while SOI MOSFET has a SiO2 buried oxide layer between active region and substrate, which truncates electron/hole collection path and reduces the charge collection at drain.[2] In addition, external factors such as LET value of injected particle and internal factors such as thickness of the top silicon film also seriously affect the anti-single event capability of SOI device.

In this paper, a 2D SOI n-channel transistor model is constructed in Sentaurus TCAD. Based on the analysis of basic structure of transistor in SOI technology. Collected charge is used as the figure of merit to evaluate SEE effects.

2. TCAD SIMULATION SETUP

Design parameters of the SOI transistor were chosen according to the PDK. Some important physical parameters are shown in Table 1. The buried oxide thickness and poly gate thickness are 0.1 μ m and 0.2 μ m respectively. The epitaxial layer (EPI) thickness is a variable parameter with 100nm, 50nm and 25nm.

Figure1 shows the 2D structure of SOI n channel transistor proposed in this paper and the doping concentration inside this device. The EPI thickness of this modeling is 0.1 μ m.

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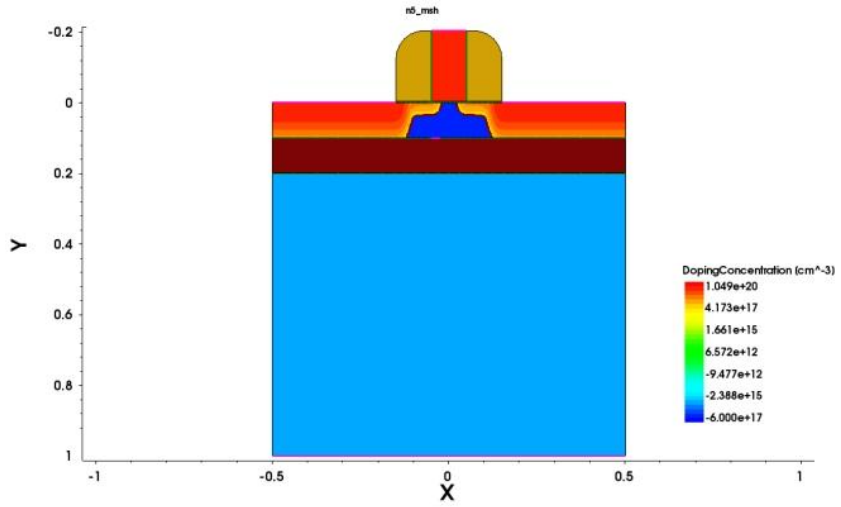

Figure 1. SOI-MOSFET structure in TCAD simulation

The IV transfer characteristic curves of SOI devices are given in Figure 2 in semi-logarithm scale. Epitaxial layer thickness of this device and Vd are respectively serve as 0.1 μ m and 0.05V. No obvious difference between tied body and floating body SOI devices due the very low drain bias limiting the avalanche and floating body effects.

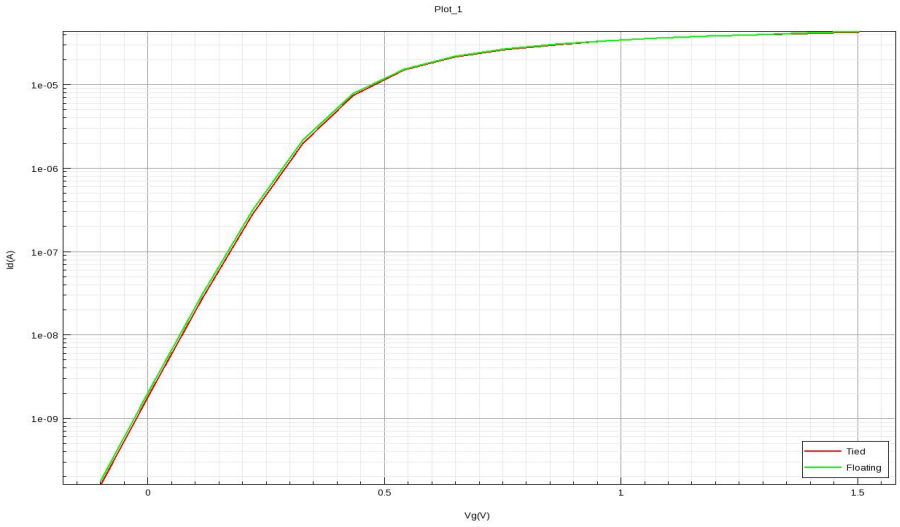

Figure 2. Id-Vg curves of tied body and floating body SOI devices

3. SIMULATION RESULTS AND DISCUSSIONS

3.1 The impacts of heavy ion LETs

If a high-energy particle is injected into depletion region of a reverse biased pn junction and substrate, silicon atoms will be ionized and generating plasma of electron-hole pairs along the path of injection particle, whose density is a few orders of magnitude higher doping concentration in substrate. This depletion region nearby the plasma is neutralized, leading to deformation of equipotential surface of electric filed in depletion region. The deforming region is always called “funnel”, which will cause a strong distortion of electric field, making the generated paired electrons and holes separate[3,4]. For nMOSFETs, holes are moved to substrate, while electrons are collected by positive electrode, which triggers SET phenomena.

With increasing of the LET values, generated ionized electron-hole pairs also grow in quantity, so more electric charge can get collected through “funnel effect”, which can widen SET pulse width and increase its peak value.

Figure 3 shows the simulation result from different LET values of 0.2pC/ μ m, 0.5pC/ μ m and 1.0pC/ μ m. The EPI thickness of device is 100nm and Vd is set as 0.1V. Device has a tied body contact. Heavy ion hits the middle of gate, which is the most sensitive region along channel length direction in terms of collected charge.[5]

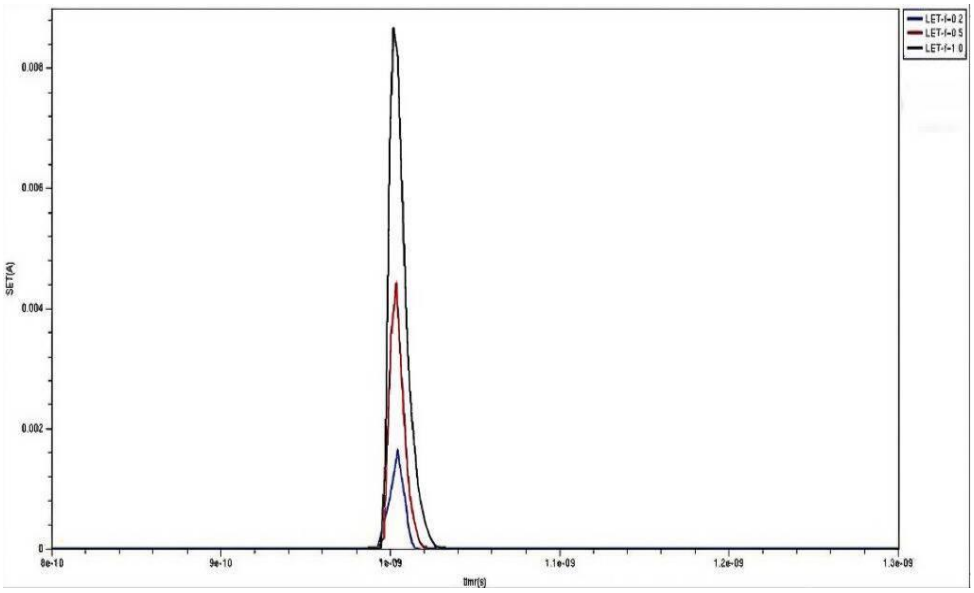

Figure 3. SET pulse at different LET values

3.2 The impacts of EPI layer thickness

Due to the presence of insulating buried oxide layer, holes generated in substrate area are impossible to be collected. The majority of excess charges collected by SOI device are generated within the top epitaxial layer. [6]For different EPI layer thickness, the corresponding SET pulse width should be different accordingly.

Figure 4 shows the simulation results with different EPI layer thickness of 25nm, 50nm and 100nm. The Vd is set as 1V and device has a tied body contact.

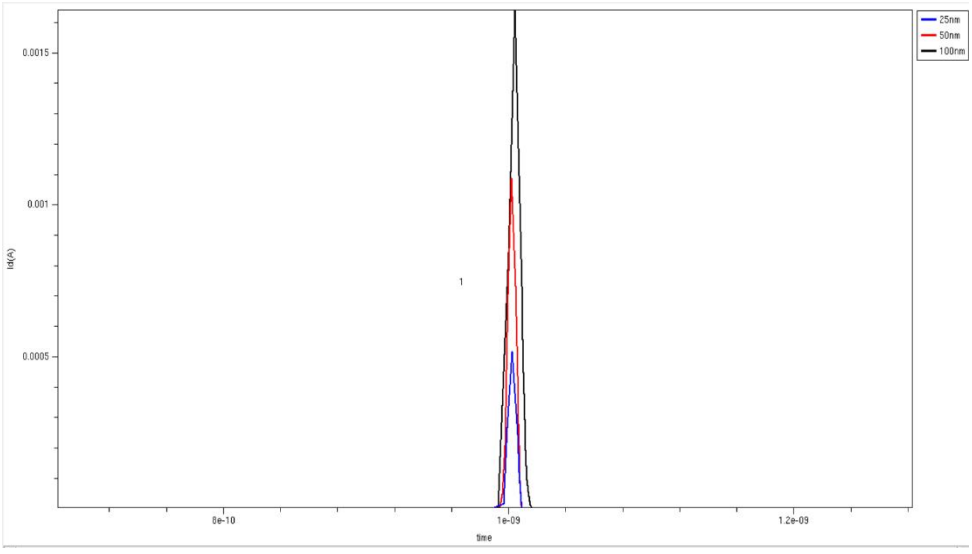

Figure 4. SET pulse with different EPI layer thickness

3.3 The impacts of body contact

In MOS structure, source-channel-drain structure is similar to an NPN bipolar transistor. High-energy particles inject into device and generate electron-hole pairs. Electrons with high mobility are instantaneously collected by drain, while the diffusion of holes towards the source region much slower, which is equivalent to the deposition of holes in the bulk region,[7] causing an instantaneous increase in bulk potential. This mechanism is called "parasitic bipolar transistor effect", [8,9]leading to the infection of carrier from source to drain and finally generating parasitic currents in drain region.

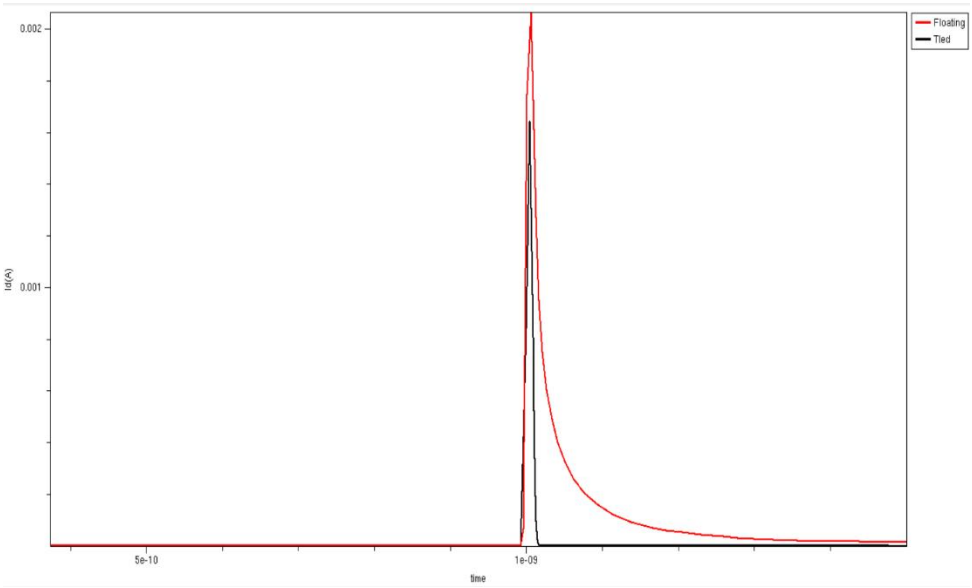

Figure 5. SET pulse with different body contact schemes

For body contact device, the equivalent base region of parasitic bipolar transistor contacts with substrate, so the excess charge within this region can be released easily, without triggering parasitic bipolar transistor. Due to the isolation by buried oxides, there is no connection between the bulk region and the external circuit, resulting in a floating potential in bulk region. When the transistor in collided by heavy ions, ionized charge cannot be removed quickly. Some electron-hole pairs recombine while other majority carriers will diffuse to source region, thereby reduce the potential of source-body junction, leading to minority carriers injected from source to bulk region and finally collected by drain.[10]

Figure 5 shows the simulation result with different body contact schemes of tied body and floating body SOI devices. The Vd is set as 1V and EPI layer thickness is 100nm.

3.4 The impacts of drain voltages

Higher drain bias can form a stronger electric field, which can collect ionized electron-hole pairs more quickly, resulting in a higher intensity of SET pulse.

Figure 6 shows the simulation result with different drain voltages of 1V and 0.05V. The EPI layer thickness is 100nm and device has a tied body contact.

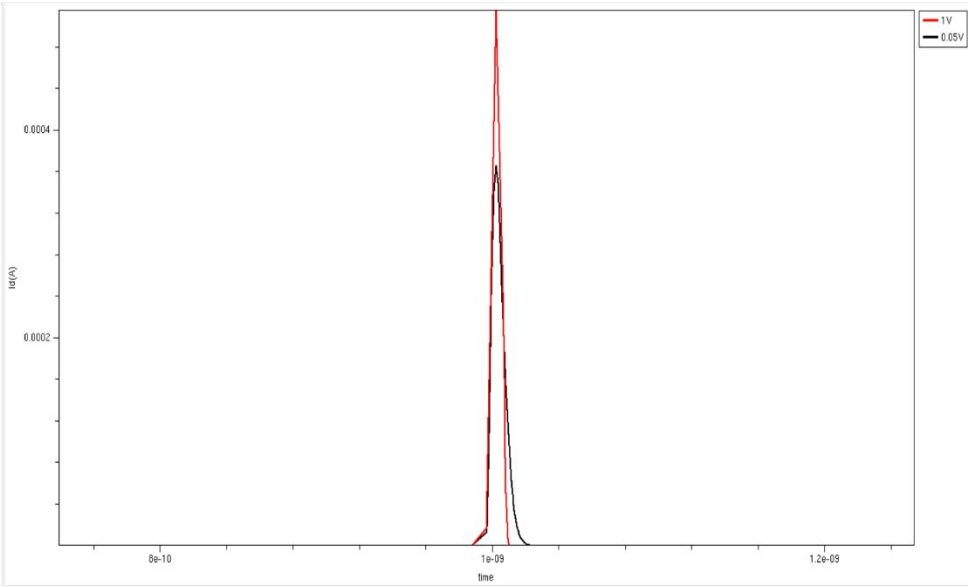

Figure 6. SET pulse with different drain voltage

4. CONCLUSION

- 2D n-channel transistor was accurately modeled in Sentaurus TCAD to simulate charge collection induced by heavy ion. Single event effect is measured by transient drain current. This paper presents an analytical model for deposited charge in SOI device based on LET value, top silicon film, bulk potential and drain voltage.
- Device with thinner top silicon film shows better anti-SEE performance by limiting the charge-generation volume.
- Floating bulk potential of SOI MOSFET degrades anti-SEE performance. If we don't take effective measures, such as connecting bulk potential to ground, bipolar amplification of parasitic transistor will offset the anti-SEE advantages of SOI devices.
- Higher drain voltages are accompanied by higher SET pulses, which challenge the circuit working conditions in harsh radiation environment.

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