Challenges for 1X nm Device Fabrication using EUVL: Scanner and Mask

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Abstract

EUVL lithography using high resolution step and scan systems operating at 13.5nm is being inserted in leading edge production lines for memory and logic devices. These tools use mirror optics and either laser produced plasma (LPP) or discharge produced plasma (DPP) sources along with reflective reduction masks to image circuit features. These tools show their capability to meet the challenging device requirements for imaging and overlay. Next generation scanners with resolution and overlay capability to produce 1X nm (10 nm class) memory and logic devices are in preparation. Challenges remain for EUVL, the principal of which are increasing source power enabling high productivity, building a volume mask business encouraging rapid learning cycles, and improving resist performance so it is capable of sub 20nm resolution.

1. ROADMAPS

Performance improvements and density increases continue in memory and logic devices driven by the lithographic shrink. Moore's Law can be expected to extend to 2018 at least. In Table 1 the general device roadmap for logic, DRAM, and flash memories is shown. This information is based on projections by device engineers at IMEC and ASML, and does not represent any specific company's roadmap. One can refer to excellent invited papers published at IEDM and the VLSI Symposium in recent years to get an in-depth view of likely developments in electron devices for the rest of this decade. (1,2,3)

Briefly, in logic, the planar CMOS transistor will be replaced by the finFET (4) or one of its variants such as the trigate transistor (5) in order to improve device leakage and drive current at smaller feature sizes. In DRAM, the storage capacitor becomes more difficult to scale and DRAM may be replaced by other devices such as the STT MRAM (6) or the Phase Change RAM (PCRAM, 7). In flash, the floating gate device faces scaling challenges in the diminishing number of electrons that constitute a bit and cell-to-cell interference. Possible replacement devices include the BiCS-type charge trap 3D stacked memory (8) and the 3D cross-point ReRAM (9). Further cost reduction in nonvolatile memories may be achieved by 3D stacking of layers such as the crosspoint concept. Further integration of different device types using through-silicon-via (TSV) technology may come to pass (10).

Lithographic shrink remains the key driver of cost reduction in almost all scenarios. Figure 1 shows the average shrink rate for each major device type as reported to ASML by its customers projected to the end of the decade. Flash memory due to its simple periodic patterns allowing full utilization of low k1 imaging and double patterning (11) has shrunk faster than other types. With more complex imaging problems, DRAM and logic have approximately the same shrink rate, with logic offset by about 18 months from DRAM. Also shown is the rate of introduction of new lithographic resolution by ASML in dry ArF, immersion ArF, and now EUV scanners to support the fabrication of these devices. 193nm immersion and multiple patterning can support 2X nm device manufacturing but at expense of excessive design rules, extended cycle times, and extreme mask complexity. EUVL shows the promise of succeeding 193nm as the main lithographic technology for 1X nm device fabrication.

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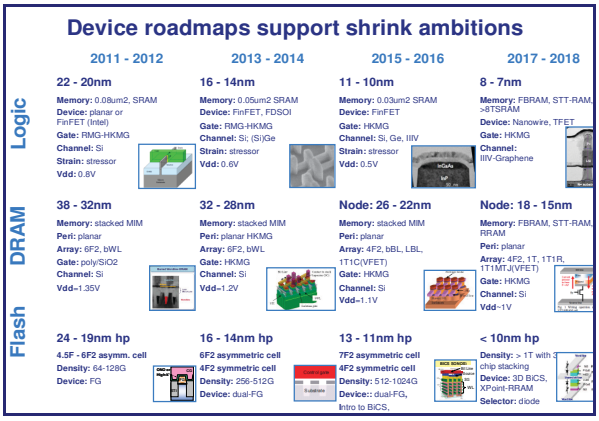

Table 1:Device roadmaps support shrink ambitions (Source: IMEC, ASML TDC)

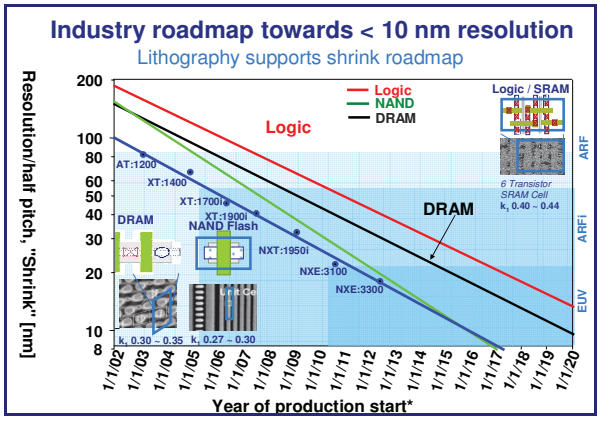

Figure 1: Industry roadmap towards < 10 nm resolution (Note: Process development 1.5 ~ 2 years in advance)*

Table 2 indicates the EUV scanner roadmap for industrialization. ASML built two development tools in 2006 which feature 0.25 NA, 6 mirror projection optics and use discharge produced plasma (DPP) sources (12). These tools have been used to produce early device demonstrations, and to allow resist chemistry and EUV mask developments. In 2010, ASML shipped the first NXE:3100 EUV scanner (13) to a chipmaker. This tool also uses the 6 mirror, 0.25NA design but due to significant improvements in mirror polishing and tool stability, the resolution achieved is substantially better. The NXE:3100 is configured to work with either DPP or laser produced plasma (LPP) sources. Six of these tools have now shipped to device makers and research institutions as of 2011. In 2012, ASML will start to ship the NXE:3300, featuring a 0.33NA projection lens. The NXE:3300 will support 1X nm device manufacturing, with expected production insertion in 2013-2014.

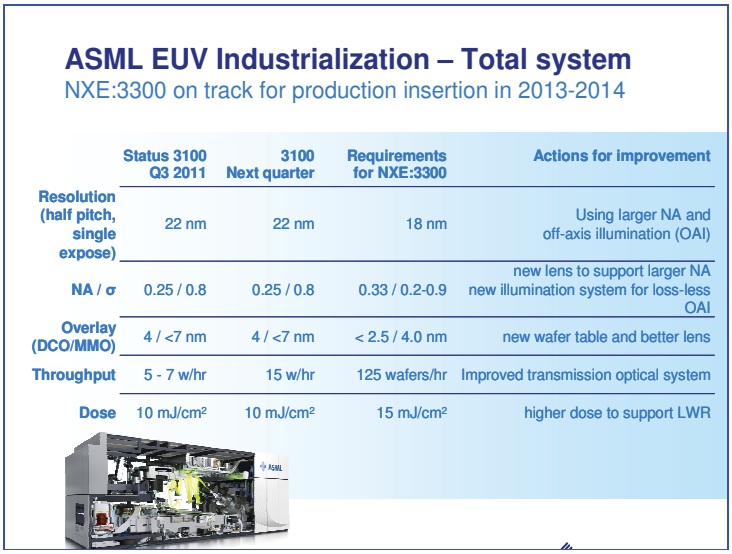

Table 2: ASML EUV Product Roadmap

2. 1X NM DEVICE REQUIREMENTS FOR LITHOGRAPHY

A trend in logic that has significant impact in lithography is the movement toward gridded layouts with restricted design rules. Mark Bohr of Intel has illustrated this (14) in gate mask layout, contrasting the style used for 65nm node with the style at 32nm (see Figure 2). On the left, the layout style for 65nm has geometries which run both horizontally and vertically, and the gates have different widths and are on different pitches. On the right, the style for 32nm features gates of uniform dimensions and oriented in one direction only. Gates are patterned as lines and spaces and then cut in a separate mask or masks. Yan Borodovsky of Intel has introduced the concept of complementary lithography which takes this trend a step further and adapts this style to interconnect layers (15). He has shown how 193nm immersion lithography can be adapted to produce 14nm node and even 10nm node logic devices using spacer technology (also known as pitch division) to pattern a very fine grating and then create openings with a number of cut masks. This elegant scheme allows 193nm immersion lithography to be extended far beyond where it was once imagined possible. However, the number of masks required to fully pattern one critical layer can be daunting: a mask to create the grating, two or more cut masks depending on the minimum pitch, and a mask (or masks) to form peripheral circuitry. How much simpler it is to consider doing this in a single exposure with EUV! Or, if LWR or line end shortening exceed budgets, EUV can be used to expose the cuts in a single exposure with much greater fidelity than would be possible with immersion scanners. Borodovsky has remarked that this method also relaxes the control needed for mask defect density due to the much lower open area in a cut mask compared to a full interconnect mask.

A similar problem for logic devices is the explosion of mask count to pattern critical contact and via layers. As the SRAM cache horizontal and vertical pitches shrink from 28nm to 20nm to 14nm node, the number of masks required to pattern the contact layer grows from one to two to three. This is seen in Figure 3 (work from joint collaboration between IMEC and ASML – ref. 16). Considering that there can be several such critical layers in the most advanced logic devices, this can add extraordinary cost and cycle time to the manufacturing process. Again, the need for a direct EUV single exposure is very apparent.

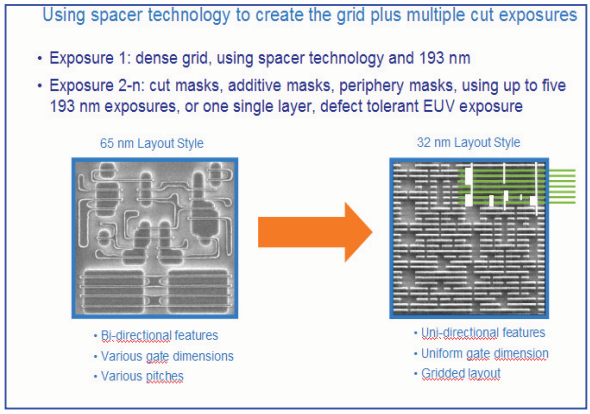

Figure 2: Design restrictions required for 193 nm extensions (14, 15)

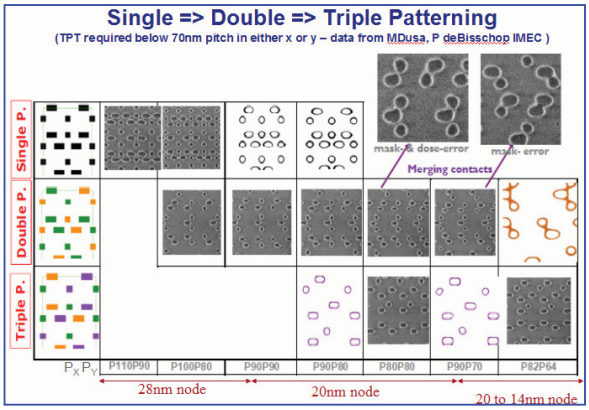

Figure 3: SRAM contact scaling with 193i (16)

In memories there are similar considerations that drive the transition from immersion to EUV. In the floating gate NAND flash memory, below 19nm node, the chipmaker must use quadruple patterning (QPT) with immersion to pattern the wordline layer. The consequences of this are shown in Table 3 which contrasts the expected CDU and LWR budgets, as well as the number of masks and process steps required for the following lithographic options: EUV SE, EUV + SPT, and ArFi QPT, both positive and negative tone. In QPT, there are three separate CD populations within a repeating range of 8 wordlines which can lead to very significant device performance issues. Up to 4 masks may be required to form the layer: two sacrificial masks plus two trim masks to take away undesired spacer features. Compared with a single mask and etch for high NA EUV this is very unattractive. However, the

NAND roadmap has been so aggressive that EUV is not yet ready to deliver the required resolution in a single exposure while 15nm class NAND may already be on the market in 2012. However, EUV + SPT can deliver the required resolution.

Finally, as in logic, EUV is an attractive technology for patterning small densely packed contact holes in the NAND flash. Figure 4 shows that 0.25NA EUV can easily resolve 30nm holes on a 40nm staggered pitch with a good process window of > 100nm DOF and > 16% EL.

CDU and Overlay Error budgets for process options for 15nm HP NAND Wordline (WL) mask

Process option	Litho HP (nm)	Line CDU (nm)			Space CDU (nm)			LWR	No. of masks/ process steps
EUV SE	15	1.5			1.5			4	1/ 2
EUV SPT	30	1.3			1.8, 3.0			2	2 / 7
ArFi +DSPT	60	1.5			1.8	2.5	3.6	2	4 /12
ArFi - DSPT	60	1.8	2.5	3.6	1.5			2	4/ 17

Multiple CD populations for spacer double (SPT) and quadruple (QPT) patterning have complex process implications and limit performance

Table 3: CDU andLWR budgets for process options for 15nm NAND Wordline (WL) mask

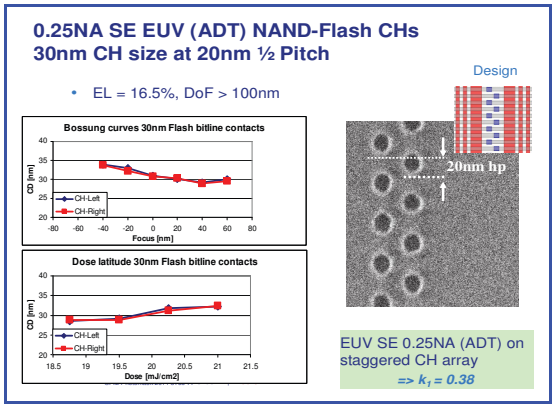

Figure 4: 0.25NA SE EUV (ADT) NAND-Flash contact holes

3. NXE:3100 EUV SCANNER IMAGING, OVERLAY, AND PRODUCTIVITY

NXE:3100 imaging has been tested in chemically amplified resist (CAR). Examples here use Shin-Etsu SEVR-140, 50nm thick, developed in standard TMAH. Figure 5 shows the process windows for 21 and 22nm lines and spaces, using full aperture of 0.25 and dipole illumination. Depth of focus of 150nm and 200nm and exposure latitudes of 8% and 12%, respectively, are achieved at doses of 17.5 and 14.5 mJ/cm2. Imaging in a unique inorganic negative-tone material supplied by Inpria (17), resolution down to 18nm L/S is achieved, however at a much higher dose (~70 mJ/cm2). These results show excellent single exposure (SE) resolution extension compared to 193nm immersion where the SE imaging cutoff is around 37nm L/S for the highest available NA of 1.35.

Resist will continue to play a key role in enabling EUVL. Images in the Inpria material exposed on the MET tool at Berkeley at 0.3NA show modulation down to 12.5nm L/S (Figure 6 left). On the right in Figure 6, 15nm L/S are produced using a spacer double patterning (SPT) process in which the NXE:3100 did the sacrificial exposure at 30nm L/S in CAR (18). SPT has the advantage of improving the initial linewidth roughness of the pattern in resist and because the first exposure is done at a reasonably large size, the dose is relatively modest (12 mJ/cm2).

Overlay on the NXE:3100 has been tested. Overlay to a dry ArF scanner shows less than 7nm overlay over 4 wafers (see Figure 7 left). This type of test is a realistic method to gauge the ability of the EUV tool to be used in a mixed fab environment where the starting layer in the process is typically done with dry ArF. On the right in Figure 7, the ability of the tool to overlay to itself is tested using dedicated chuck overlay, or DCO (NXE:3100 is a dual stage system as in the TWINSCAN platform used for KrF and ArF scanners. In DCO the wafer has both layers exposed on the same chuck). These results indicate DCO of less than 4nm is achieved over two wafers.

So, the imaging and overlay are good, and supports the requirements for device fabrication. This allows chipmakers to use these tools to learn and develop their processes and prepare for inserting EUV into high volume production in the 2013 and 2014 time frame. For that they need to expose more wafers per hour and we need a more powerful light source. We are working with three EUV source suppliers, Cymer, Gigaphoton, and Ushio. The first two are developing laser produced plasma (LPP) sources, while the third is developing a discharge produced plasma (DPP) source. Figure 8 shows photographs of these three sources. The tool can now produce throughputs in the mid-teens

per hour which has been demonstrated and repeated on a fully integrated pilot system in our factory in Veldhoven. Further improvements have been demonstrated in an R&D environment at Cymer and Ushio.

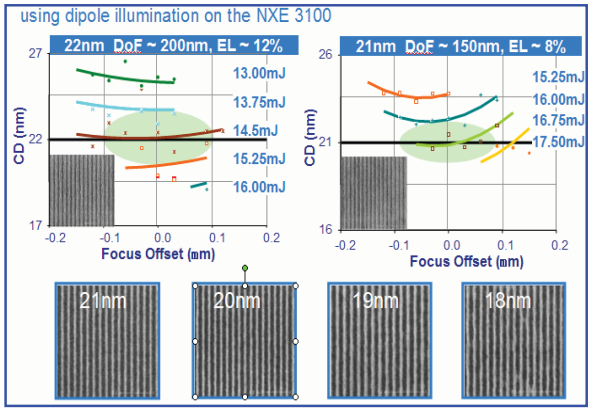

Figure 5: 18 nm imaging achieved on NXE:3100 at NA 0.25 With dipole illuminatin in negative tone inorganic resist (17). 21 nm L/S with 8% EL and 150 nm DOF in chemically amplified resist.

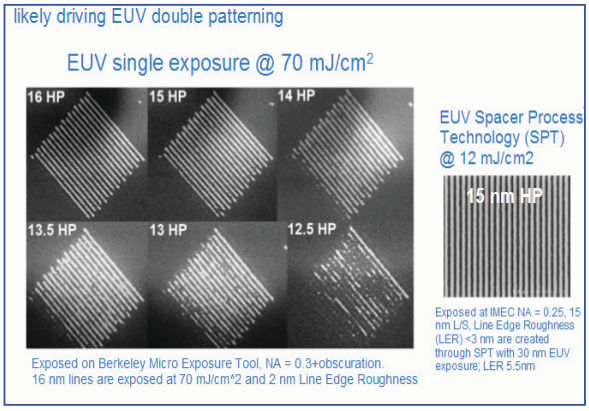

Figure 6: Extension of EUV resist is progressing but remains a challenge. High resolution shown in inorganic resist (Inpria-17). Spacer double patterning can improve linewidth roughness for 15 nm L/S.

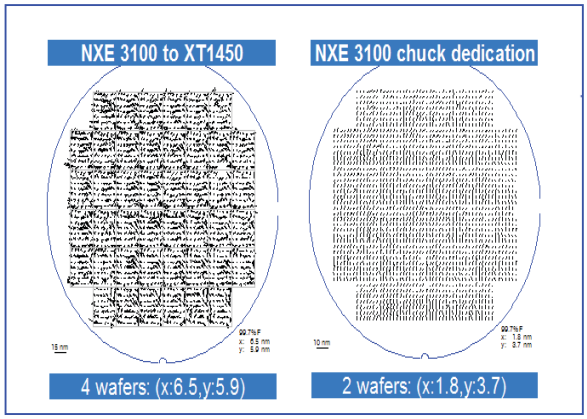

Figure 7:EUV to dry 193 Overlay measured at 6.5 nm (NXE:3100 to XT:1450)

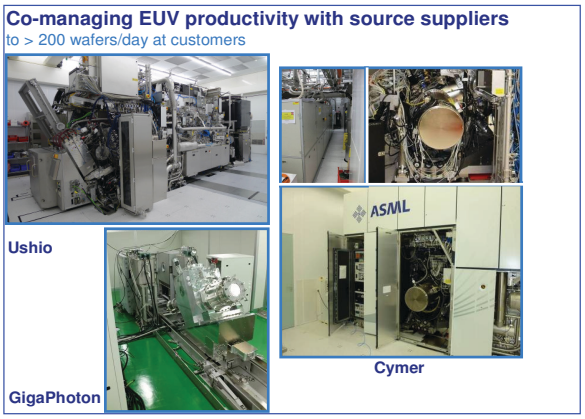

Figure 8:Co-managing EUV productivity with EUV source suppliers (Ushio DPP; Cymer and Gigaphoton LPP)

4. EUV MASKS FOR 1X NM DEVICES

EUV masks enjoy many of the same attributes as projection masks for ArF immersion lithography. They have the same dimensions and are 4X demagnified. This is very key to their eventual use as they can be written, processed, handled, cleaned, and inspected in many of the same tools as are used today in modern mask shops. However, there are several key differences as well, the most important of which is the mask is reflective rather than transmissive. The mask blank consists of many dozens of multilayers of Mo and Si deposited on a LTE substrate, constituting a Bragg reflector which achieves about 60-70% reflectivity at 13.5nm. Ta-based materials are used as an absorber over the multilayer (replacing chrome or MoSi absorber in an DUV mask). Finally, because EUV light is strongly

absorbed by most materials, there is currently no pellicle for the EUV mask which has serious implications for mask cleanliness and handling. Many of these issues are covered in other papers in this conference and will not be discussed further here.

Unique mask and scanner interactions in EUVL include shadowing and flare. Mask shadowing occurs because the light falls on the mask at an average angle of 6 degrees due to the catoptric lens design. Since the effect is easily modeled, it can be incorporated in an OPC model for mask compensation. Flare due to scattering of light from the polished mirror surfaces is also a well-understood effect. Figure 10 shows experimental measurement of flare for the NXE:3100 tool, indicating flare of under 5% for 2mm bars, substantially better than the performance of the ADT. Figures 11 and 12 show the experimental data for through slit and through scan flare for both ADT and NXE:3100, indicating an improvement of about 3X. Simulations done with Brion's Tachyon computational lithography software show excellent agreement with the data, indicating that flare is well-understood and modeled (19).

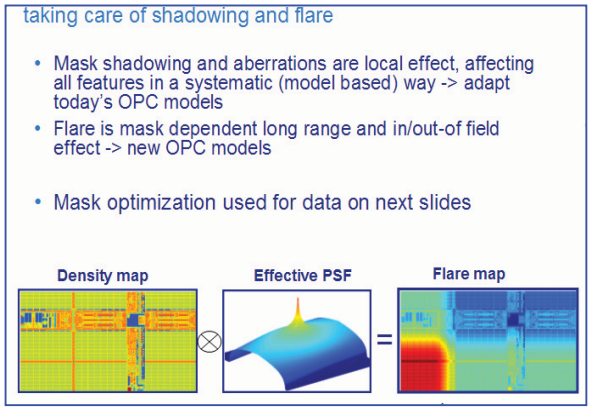

Figure 9:NXE:3100 imaging optimized with specific OPC (19)

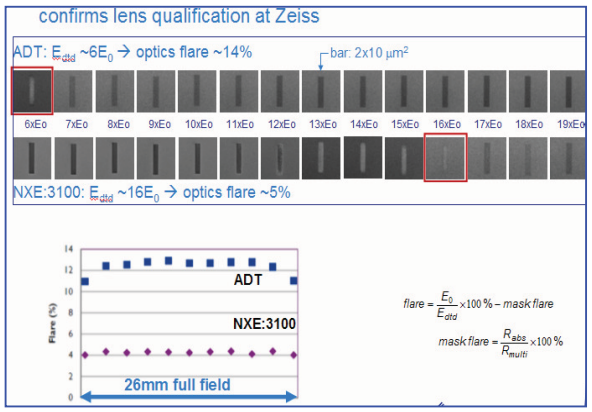

Figure 10: NXE:3100 Flare measurement is < 5% under 2mm bar (19)

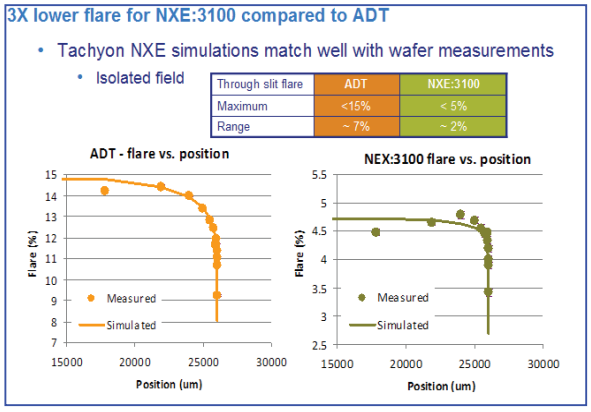

Figure 11: Through slit flare simulations vs. wafer measurements (19)

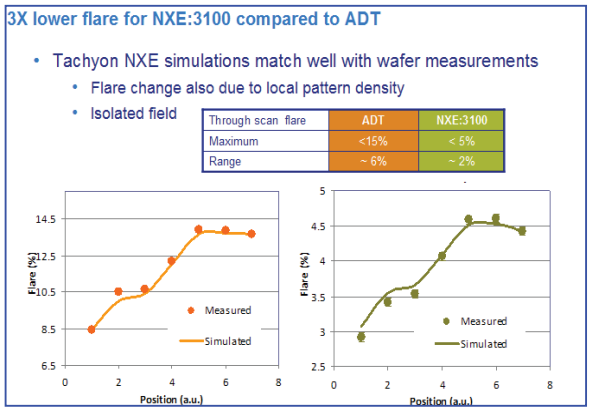

Figure 12: Through scan flare simulations vs. wafer measurements (19)

Finally, the integrated performance of optimized masks and the NXE:3100 is illustrated for several device layer examples. Figure 13 shows the 20nm NAND contact hole layer. Figure 14 shows the CD uniformity of several features in an SRAM metal 1 mask at 18nm node, while Figure 15 shows CDU for 16nm node contact holes. Figure 16 shows the imaging fidelity for contacts and metal 1 trenches for a sub 16nm node SRAM.

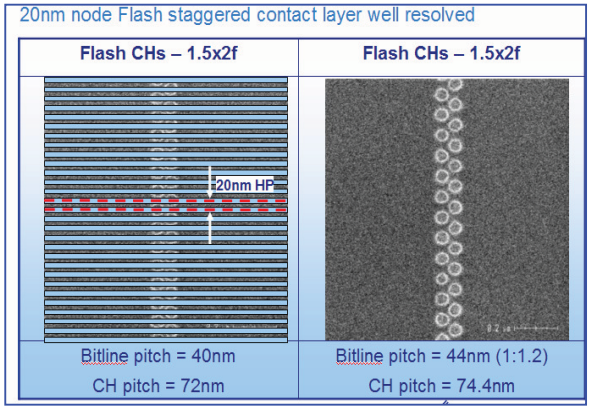

Figure 13:20 nm node flash contact layer

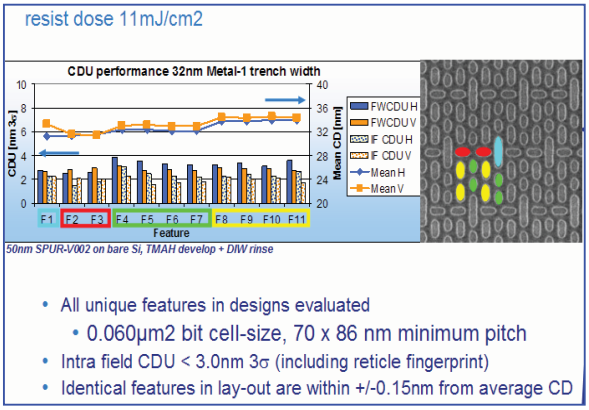

Figure 14:18nm node SRAM Metal < 3.0nm IF CDU (0.060mm2 cell)

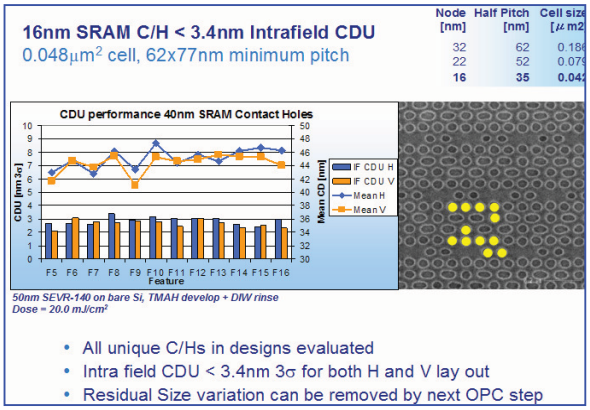

Figure 15:16nm SRAM C/H < 3.4nm Intrafield CDU

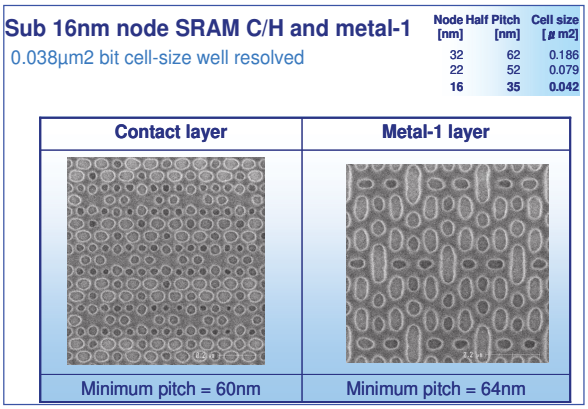

Figure 16:Sub 16nm node SRAM C/H and metal-1 exposed on NXE:3100

CONCLUSIONS

Performance improvements and density increases continue in memory and logic devices driven by the lithographic shrink. Moore's Law can be expected to extend to 2018 at least. 193nm immersion and multiple patterning can support 2X nm device manufacturing but at expense of excessive design constraints, extended cycle times, and extreme mask complexity. EUVL shows the promise of succeeding 193nm in imaging and overlay.

ASML EUV scanners are now inserted into device development lines. These tools show their capability to meet the challenging device requirements for imaging and overlay. Next generation scanners with resolution and overlay capability to produce 1X nm memory and logic devices are in preparation.

Many challenges remain for EUVL, the principal of which are

- Source power enabling high productivity
- Volume mask business encouraging rapid learning cycles
- Improved resist performance capable of sub 20nm resolution

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