Electron multi-beam technology for mask and wafer writing at 0.1nm address grid

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ABSTRACT

An overview of electron beam tool configurations is provided. The adoption of multi-beam writing is mandatory in order to fulfill industrial needs for 11nm HP nodes and below. IMS Nanofabrication realized a 50keV electron multi-beam proof-of-concept (POC) tool confirming writing principles with 0.1nm address grid and lithography performance capability. The new architecture will be introduced for mask writing at first, but has also the potential for 1xmask (master template) and direct wafer writing. The POC system achieves the predicted 5nm 1sigma blur across the 82µm x 82µm array of 512 x 512 (262,144) programmable 20nm beams. 24nm HP has been demonstrated and complex patterns have been written in scanning stripe exposure mode. The first production worthy system for the 11nm HP mask node is scheduled for 2014 (Alpha), 2015 (Beta) and 1st generation HVM mask writer tools in 2016. Implementing a multi-axis column configuration, 50x / 100x productivity enhancements are possible for direct 300mm / 450mm wafer writing.

Keywords: electron, multi-beam, mask writer, template writer, direct wafer writer, MBMW, EBDW

1. INTRODUCTION

There is increased industrial interest and demand for electron multi-beam systems in a four-fold manner: (i) Single variable shaped beam (VSB) mask writer tools cannot keep up with the exponential growth of shot numbers at substantial reduced average shot size [1]. Further, there is the need to enhance the resist exposure dose by a factor of 5 to 10 to $100µC/cm^2$ in order to ensure sufficiently low line edge and line width roughness [2, 3]; (ii) 193nm immersion lithography is extended to sub-15nm nodes on 300mm and 450mm wafers. Though, in combination with self-aligned quadruple patterning, viable solutions are established to realize 11nm HP fine-line grids, there is the need of multiple patterning with a number of masks for cutting lithography [4, 5]; (iii) With progress reported on defect reduction, imprint lithography targets single patterning for cutting lithography. For this purpose an advanced multi-beam mask writer is needed as well [6]; (iv) Ideally, a mask-less lithography technology should be offered with massively parallel electron beam direct write (EBDW). [7] In order to realize a 300mm wafer throughput of 100WPH at $100µC/cm^2$ exposure dose, a total electron multi-beam current (all beams "on") of >2mA is needed.

So far, two electron single beam writing techniques are established: (i) 50-100keV Gaussian spot beam (SB) tools providing sub-10nm resolution at very low throughput with 0.1-1nA beam current, and (ii) 50keV variable shaped beam (VSB) tools, providing up to $400A/cm^2$ current density [8] with average 0.1µA current.

There are several proposals on how to realize a break through multi-beam (MB) column solution which can provide 10x – 40x more beam current than the most advanced VSB tools (Fig. 1): (i) A slim (ca 20mm diameter) column providing a fixed shape beam as proposed by Multibeam Corporation for complementary electron beam lithography (CEBL) with the argument that cutting needs to be done on 5% of the 300mm wafer area and a single beam shape is sufficient [9]; (ii) A multi-column cell (MCC) approach as pursued by Advantest, using VSB combined with character projection in each cell to improve throughput [10]; (iii) A multi (variable) shape beam (MSB) column as proposed by Vistec [11]; (iv) The IMS Nanofabrication column with a blanking device and projection optics with 200x reduction [12]; (v) A reflective electron beam lithography (REBL) configuration as pursued by KLA-Tencor [13].
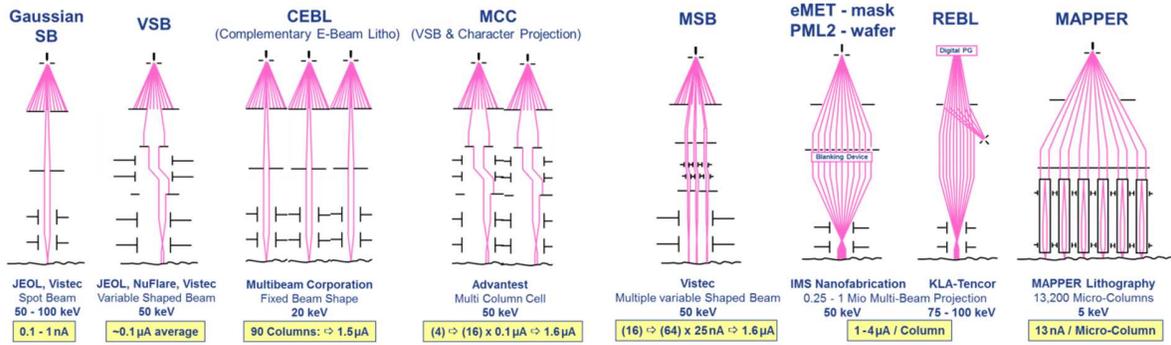
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Figure 1: Overview of proposed multi-beam configurations
(eMET: electron mask exposure tool, PML2: projection mask less lithography, REBL: reflective electron beam lithography)

In order to reach the 2mA beam current, however, as needed for 100WPH EBDW an additional productivity enhancement by more than 3 orders of magnitude is needed as shown in Figure 2: First, the 1-4µA MB column needs to be sufficiently small so that 50-100 columns can be placed on the area of a 300mm wafer and thus ca 200µA beam current can be achieved. Second, 10-20 multi-column tools need to be clustered to realize the targeted >2mA total beam current required for 100WPH EBDW.
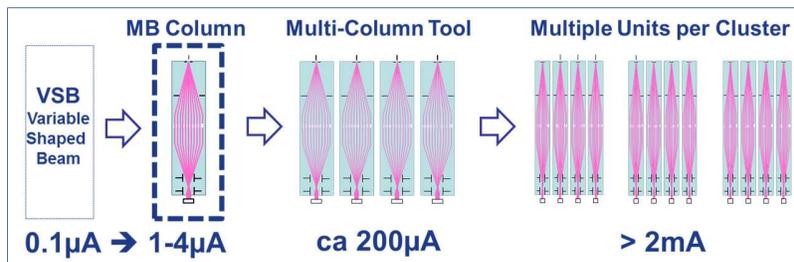

Figure 2: Evolution of electron beam systems as needed to realize 100WPH EBDW

For REBL, there is the KLA-Tencor proposal [13] to realize a multi-column tool configuration with 36 columns exposing 6 wafers in parallel, and to cluster such tools to reach the 100WPH EBDW target (Fig.3). In the MAPPER approach there is the target to realize 13,200 micro-columns within an area of 26mm x 26mm and to have 49 programmable beams within each micro-column which hit the wafer substrate at 5keV beam energy. [14] With each micro-column providing 13nA, the targeted multi-micro-column tool current is ca 170µA. There is the target to cluster 10 micro-column tools to reach 1.7mA beam current.
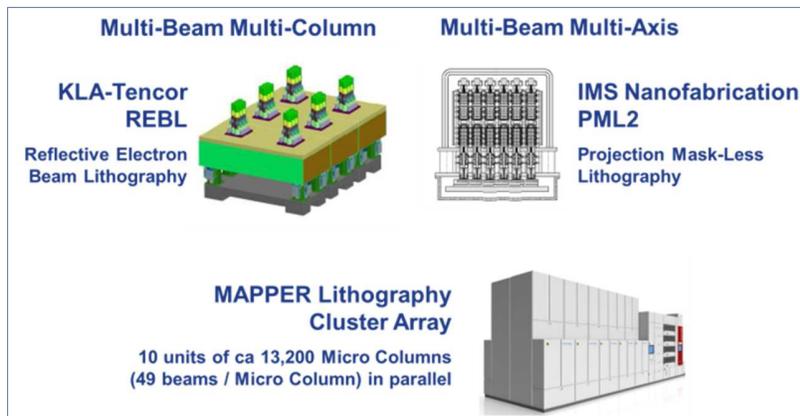

Figure 3: Schematics of REBL, PML2 and MAPPER multi-column / cluster tool configurations

IMS Nanofabrication is fully focused on the commercialization of its novel 50keV electron multi-beam solution which provides 1-4μA total beam current. For leading-edge mask exposures already 1μA beam current is sufficient to meet the industrial needs of realizing 10h write time even when using a resist with an exposure dose of $100\mu C/cm^2$. [3]

IMS Nanofabrication's multi-beam mask writer series is called eMET, which is short for electron Mask Exposure Tool. A proof-of-concept tool (eMET POC) was realized in 2011 [3] with extensive testing throughout 2012. [15, 16, 17]

2. eMET PRINCIPLES AND REALIZED PROOF-OF-CONCEPT TOOL

The basic principles common to all eMET systems are shown in Figure 4. Electrons extracted at gun-level first pass through a multi-electrode stack, which acts as a condenser and generates a broad, homogeneous beam of 25mm in diameter. This electron beam then impinges perpendicularly onto a programmable Aperture Plate System (APS), where 512 x 512 (262,144) micrometer sized beams are formed (cf. 256k-APS). Additionally, each beam can be deflected individually by CMOS-controlled micro-deflectors. All beams (deflected and undeflected) then enter the projection optics of the system where they get accelerated from 5keV to 50keV beam energy in an electrostatic multi-electrode lens and 200x demagnified by a magnetic lens system located at the bottom of the optical column. Only undeflected beams make it to the substrate level. Deflected beams are filtered out at a stopping aperture plate in the projection optics. All eMET systems are designed to print 82μm wide stripes on-the-fly, i.e. the substrate is continuously moving at constant velocity underneath the column while beams at switched on and off according to the data fed into the APS via the eMET data path. In this write mode IMS' proprietary writing strategy provides an inherent redundancy of up to 16x. This high redundancy level averages out the effects of individual defective beams and thereby allows ignoring up to 100 (statistically distributed) defective beams. Furthermore, the operability of APS units is monitored in-situ on a weekly basis by measurements which give information on the precise position of all defective beams. This information can be used to further reduce the impact of defective beams via online correction in the eMET data path. This inherent property of the eMET writing strategy coupled with the online correction capability drastically reduce the technical risk associated with the most critical element of this new technology and speak for the suitability of IMS' multi-beam solution for high-volume manufacturing.
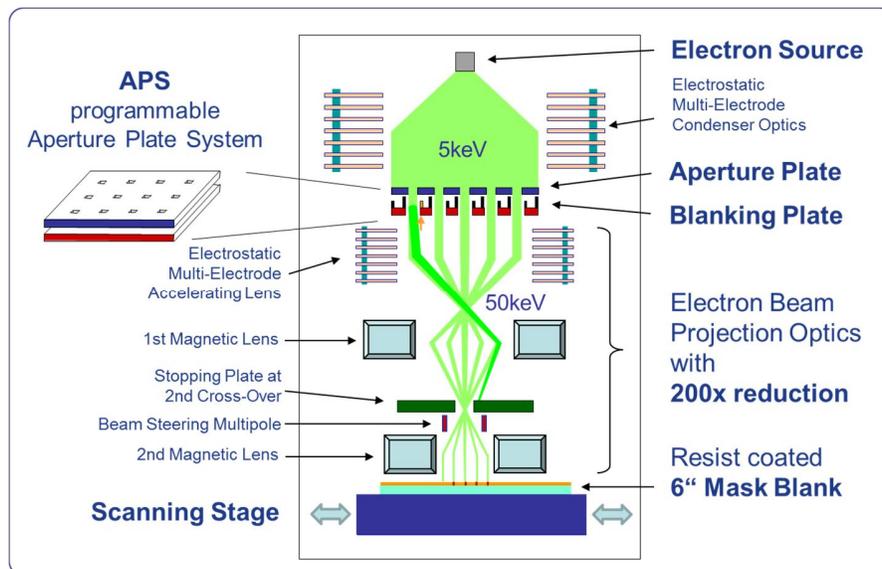

Figure 4: eMET Principles

In 2011 a first Proof-of-Concept (POC) version – the eMET POC – was integrated and finalized based on a tight schedule. The eMET POC was designed from scratch to meet all lithographic requirements of the 11nm HP node such as resolution capability (i.e. minimum feature size), pattern fidelity, critical dimension uniformity (CDU), line width roughness (LWR), registration etc. within 1cm x 1cm fields on 6 inch mask blanks. The fully integrated eMET POC can be seen in the left of Figure 5 during 2012 factory acceptance tests at IMS Nanofabrication in Vienna, Austria.
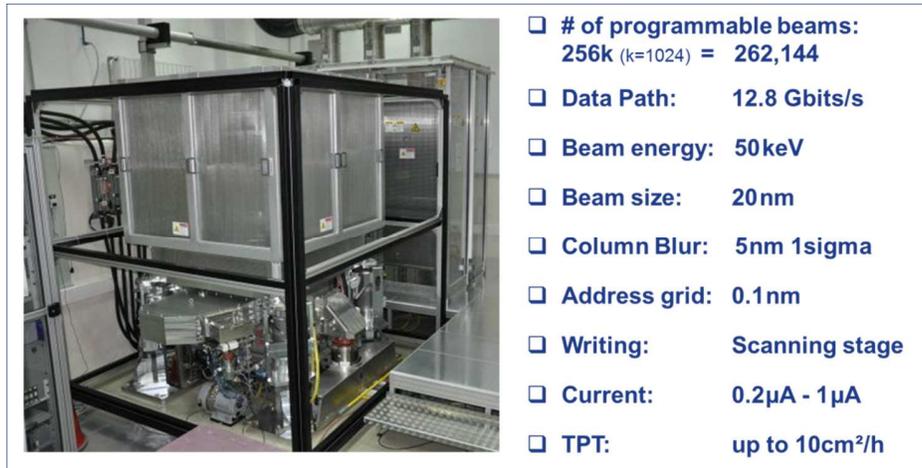
Figure 5: eMET POC during factory acceptance tests at IMS Nanofabrication, Vienna, Austria and main specifications.

Using 0.25µm CMOS technology a blanking plate was realized with 512 x 512 = 262,144 apertures of 4µm x 4µm opening size and 32µm pitch between the apertures within a ca 16.4mm x 16.4mm field. With 200x reduction of the electron projection optics, 256k (k=1024) programmable beams of 20nm beam size are projected at 50keV beam energy to the 6" mask substrate within a ca 82µm x 82µm beam array field. Monitor exposures were done on resist coated 150mm Si wafers. With this novel electron multi-beam optics a very low column blur of ca 5nm 1sigma was verified []. Very low resist blur was added when using HSQ (Hydrogen Silsesquioxane) negative resist which needs a very high dose of ca 1000µC/cm^2.

First eMET POC results are reported here with exposures on 6" mask blanks in a production worthy insensitive positive chemically amplified resist (pCAR).

3. eMET POC EXPOSURE WITH 0.1 NANOMETER ADDRESS GRID

Using MESA (Multiple Exposure Shot Addressing) techniques [xx] with 20nm beam size, there is the possibility, using overlapping shots, to expose on a 5nm physical grid such that the line edge can be placed on a 0.1nm address grid (Fig. 6a) with deviations as small as ± 50pm (Fig. 6b). The simulated exposure latitude with respect to edge position is 1.06nm ± 0.02nm for 10% change of dose as shown in Figure 7c.
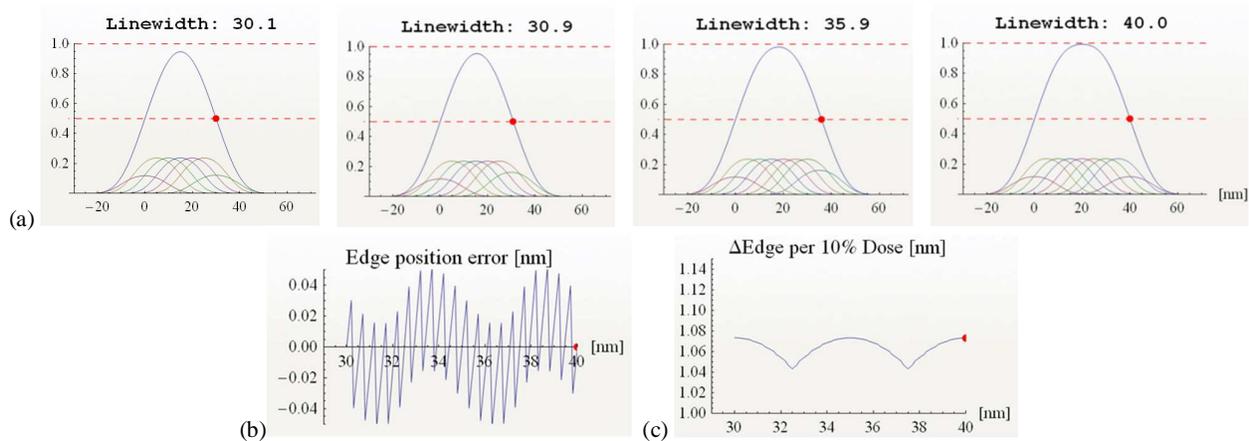

Figure 6: (a) Simulated change of edge position in 0.1nm steps showing several examples between 30.0nm and 40.0nm; (b) Simulated deviation of edge position from 0.1nm address grid; (c) Simulated change of edge with 10% change of dose vs. line width.

A rigorous experimental study was done by printing 50nm vertical and horizontal lines with pitch values varied between 100.0nm and 109.9nm in steps of 0.1nm. Such exposures were done in HSQ negative resist as well as in pCAR positive resist (Fig. 7). In both cases there is a linear relationship between CD-SEM measured pitch vs. design pitch with 3sigma deviations as low as 0.23nm and 0.30nm, respectively. The CD value 3sigma variations are 1.6nm and 1.5nm, respectively. These experimental results demonstrate the capability of multi-beam writing with 0.1nm address grid.
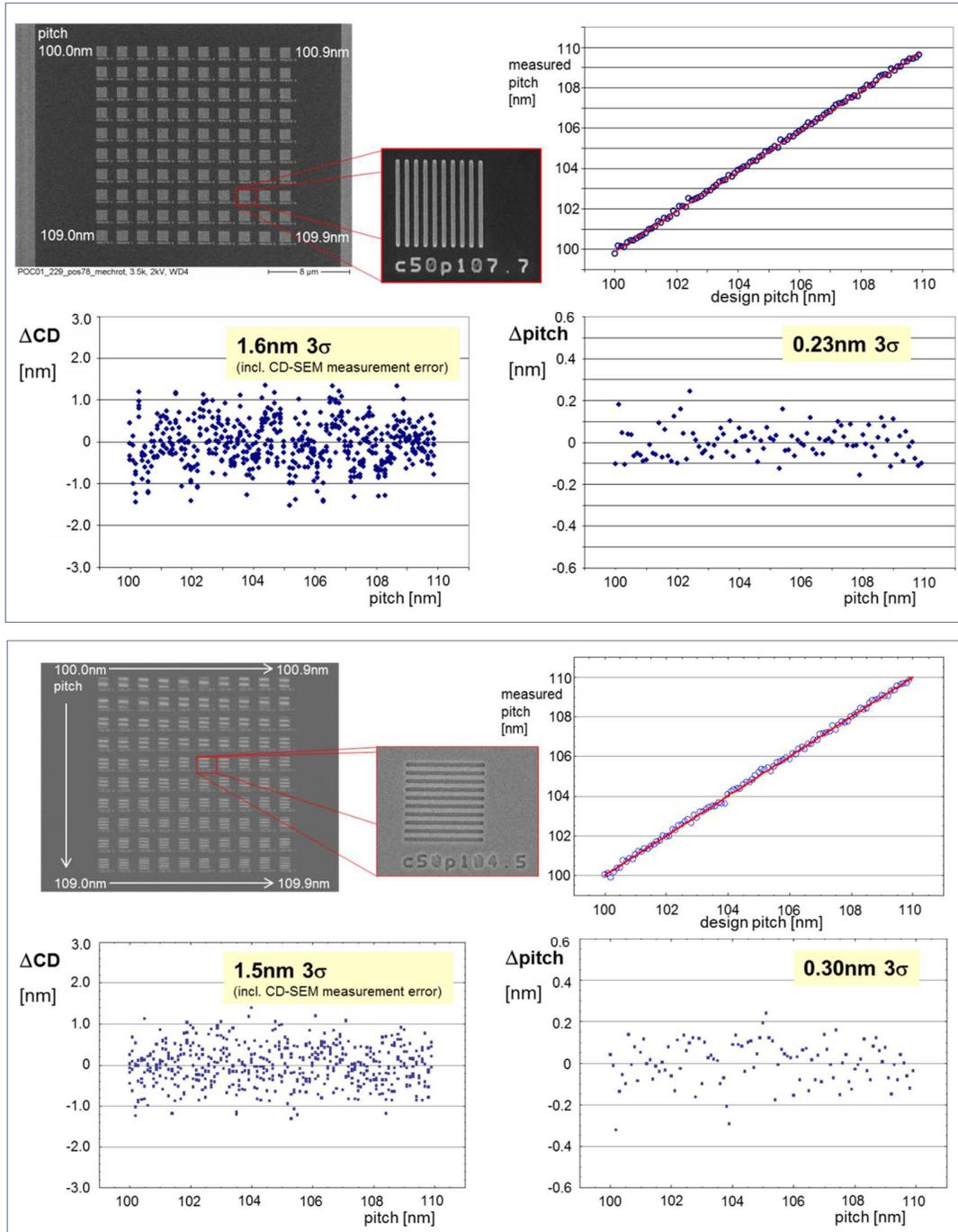

Figure 7: eMET POC exposure of 50nm lines whose pitch was varied between 100.0nm and 109.9nm in 0.1nm steps; vertical lines in HSQ negative resist and horizontal lines in pCAR positive resist. The line width and pitch values are written with 30nm line width.

A further study of multi-beam printing was done by exposing 40nm dots in HSQ negative resist (i) with 80nm pitch and (ii) with 81nm pitch. There is no change of the 1.6nm 3sigma local CDU value when placing the dots at grid positions different from the 5nm physical grid as shown in Figure 8.
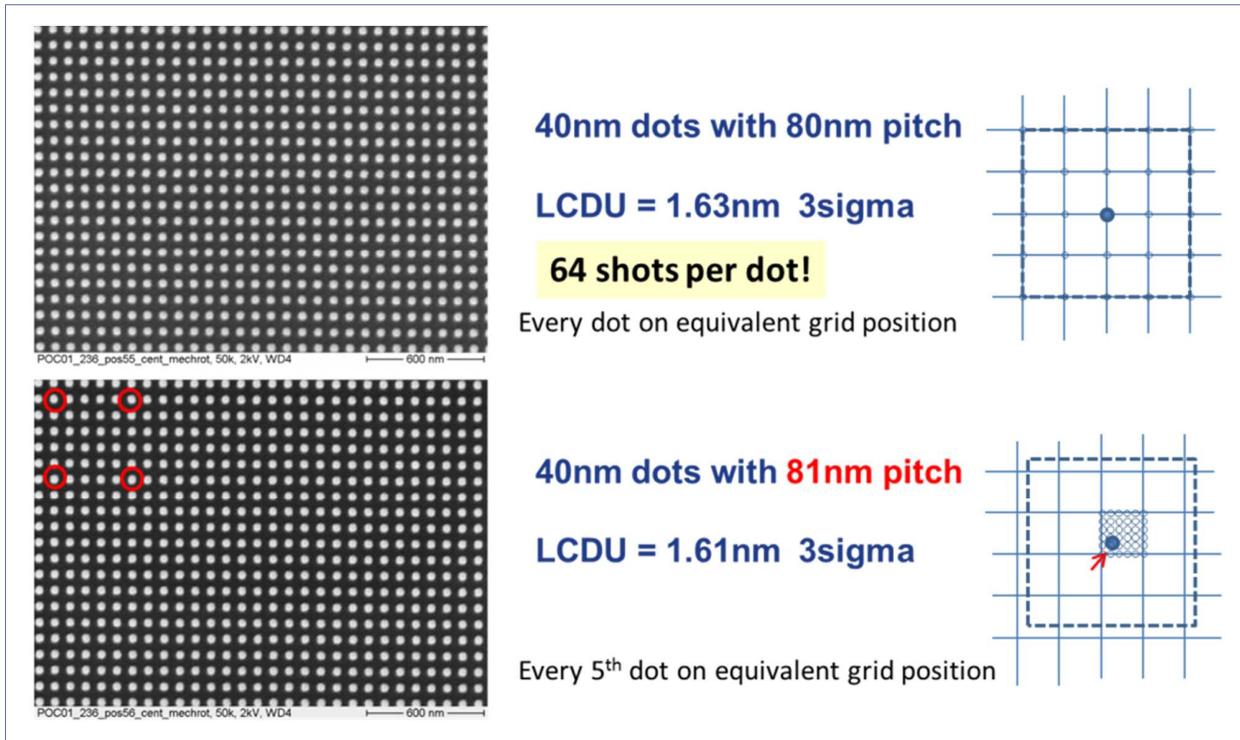

Figure 8: eMET POC exposure of 40nm dots in HSQ negative resist with 80nm pitch (above) and 81nm pitch (below).

There is the possibility to realize improved corner rounding (Fig. 9) by placing serifs at the corners (Fig. 10). According to MESA techniques there is no throughput degradation when inducing such pattern exposure improvements.
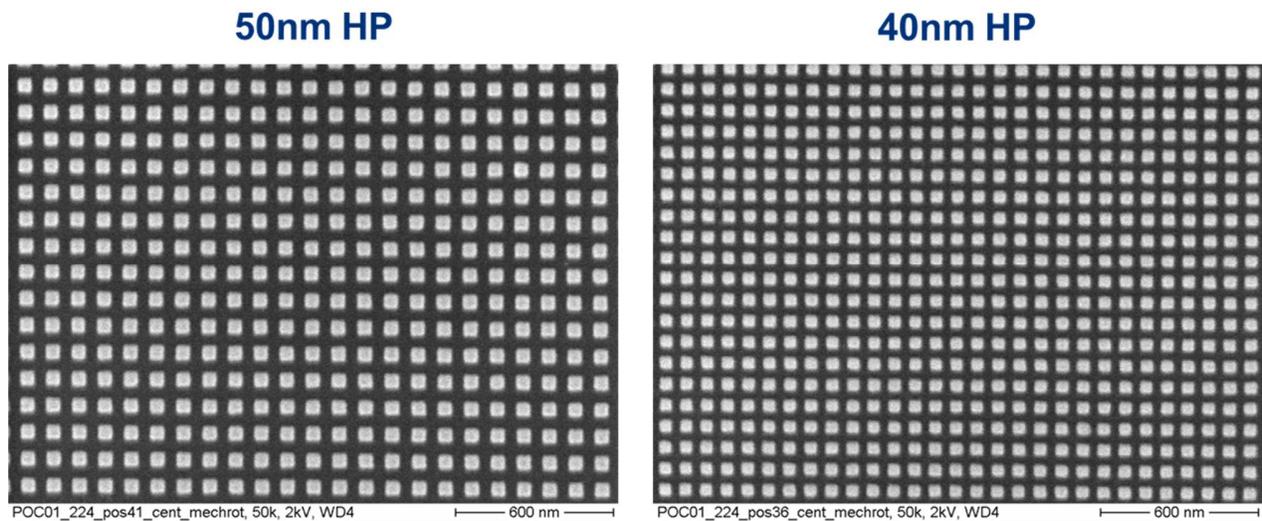

Figure 9: eMET POC exposure of 50nm HP dots and 40nm HP dots in HSQ negative resist with improved corner rounding.
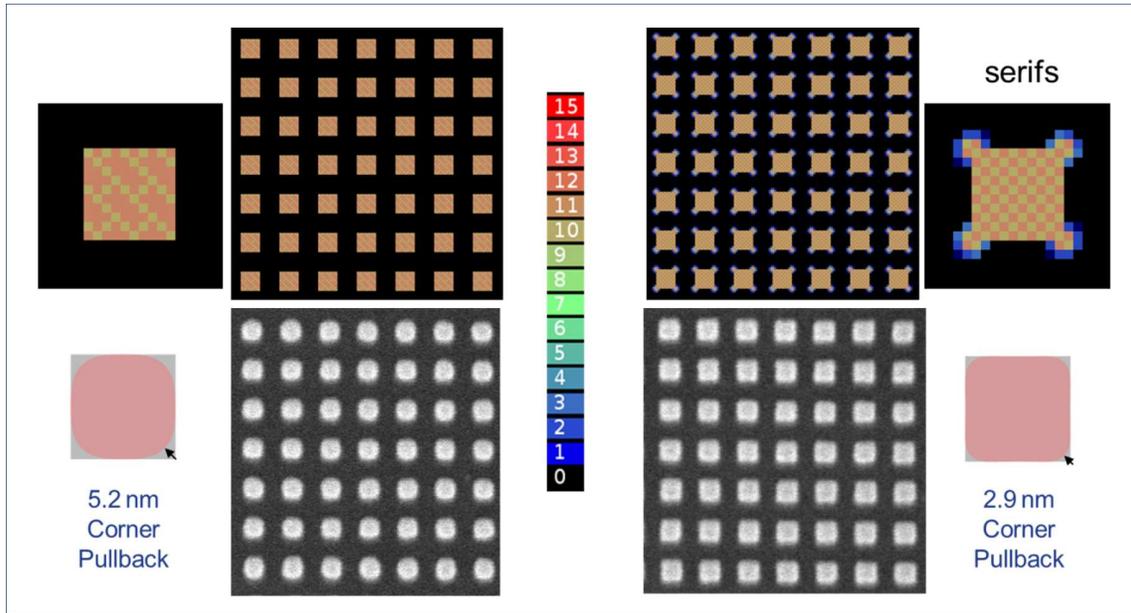
Figure 10: Bit map (above) and 50nm HP dot exposure (below) in HSQ negative resist without (left) and with (right) improved corner.

4. eMET POC EXPOSURE OF OPC AND ILT PATTERNS

There is agreement between simulation and exposure results of aggressive OPC (optical proximity correction) mask patterns in pCAR positive resist as demonstrated in Figures 11 and 12.

This holds also for the exposure of ILT (inverse lithography technology) mask patterns in HSQ negative and pCAR positive resist (Fig. 13).
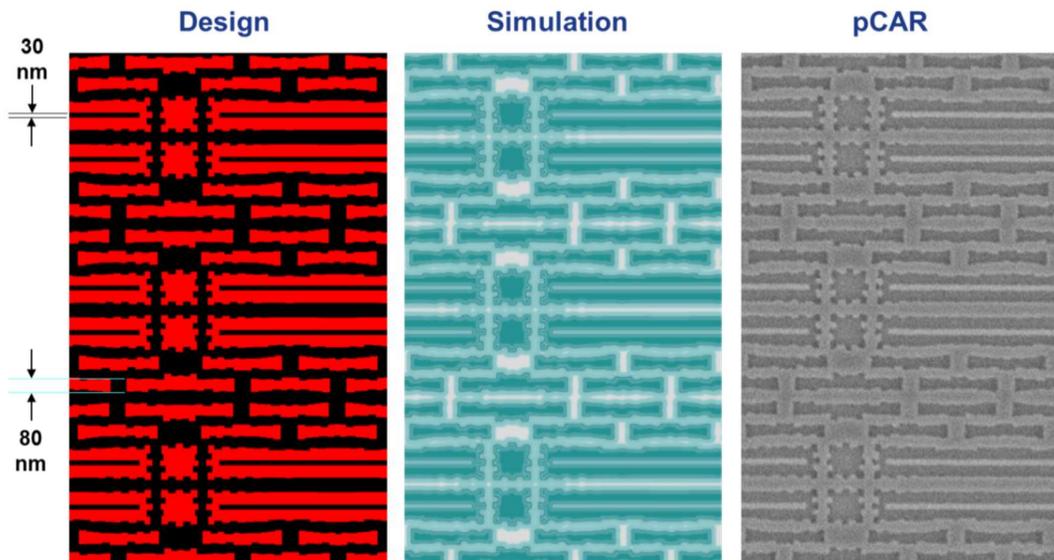

Figure 11: eMET POC exposure of aggressive OPC mask pattern in pCAR positive resist.
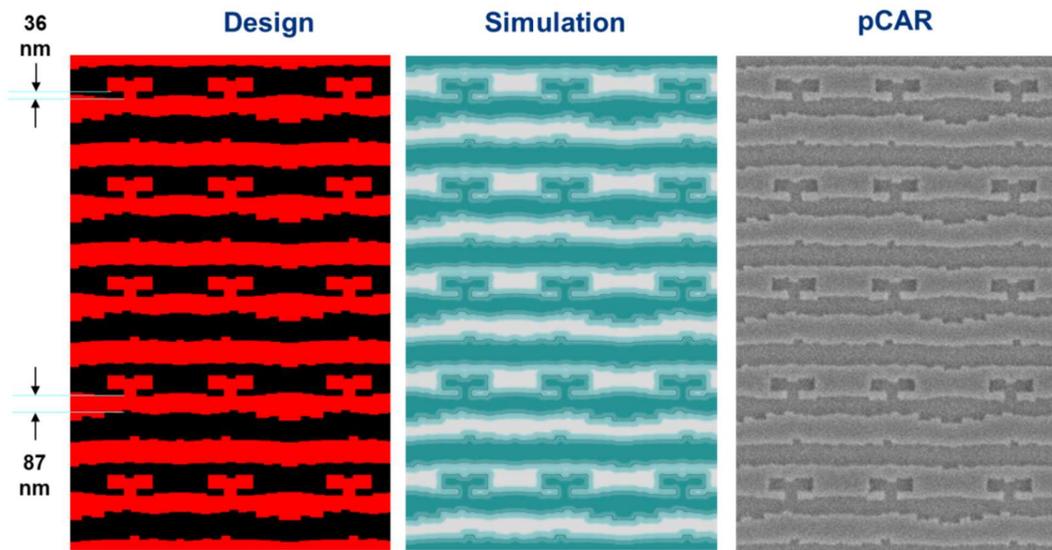
Figure 12: eMET POC exposure of aggressive OPC mask pattern in pCAR positive resist.
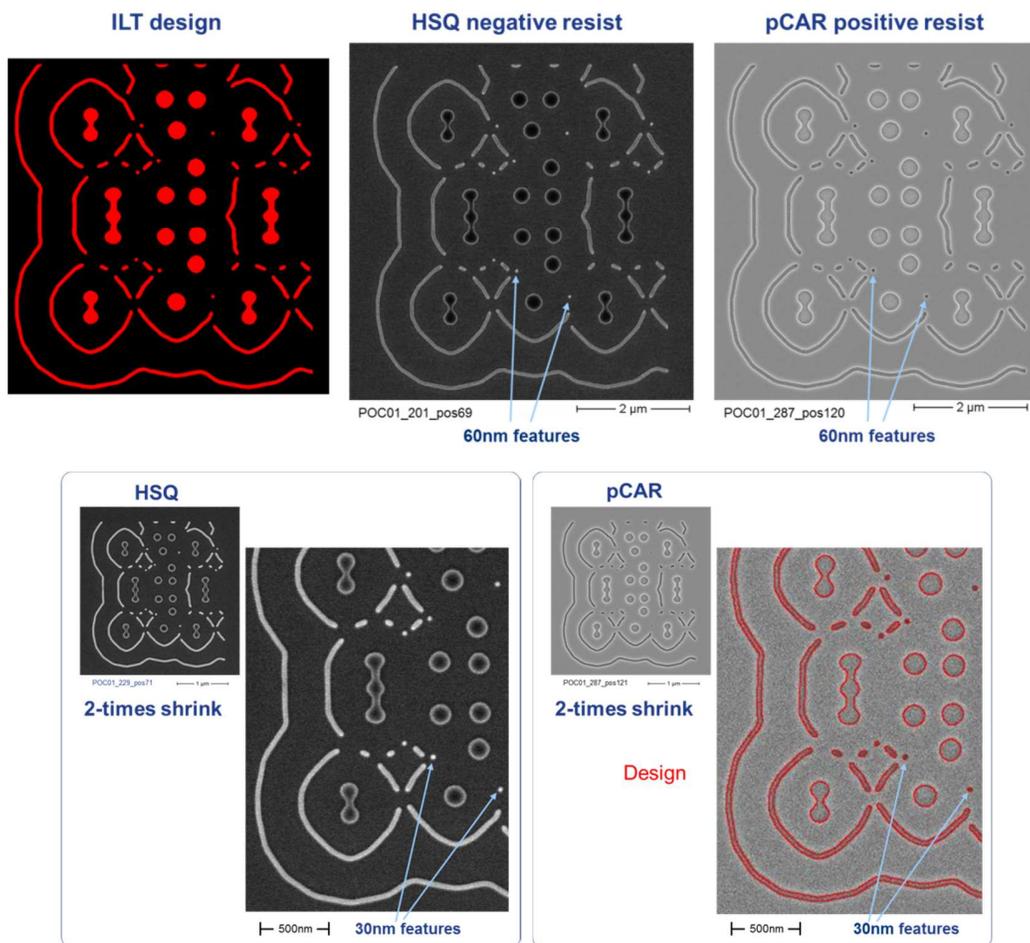

Figure 13: eMET POC exposure of ILT mask pattern in HSQ negative and pCAR positive resist.
The ILT test pattern was provided by DNP [18, 19] and was exposed according to design and also with 2-times shrink.

5. eMET POC RESOLUTION USING 20 NANOMETER BEAM SIZE

The eMET POC resolution capability, using 20nm beam size, is shown in Figure 14 with examples of 30nm HP 45°/135° as well as 24nm HP and iso lines in HSQ negative and pCAR positive resist.

(a)

(b) POC01_237_pos57_cent_mechrot, 50k, 2kV, WD4   ⊢——— 600 nm ———⊣

(c) POC01 291 pos102   ⊢——— 700 nm ———⊣   POC01_292_pos055   ⊢——— 700 nm ———⊣
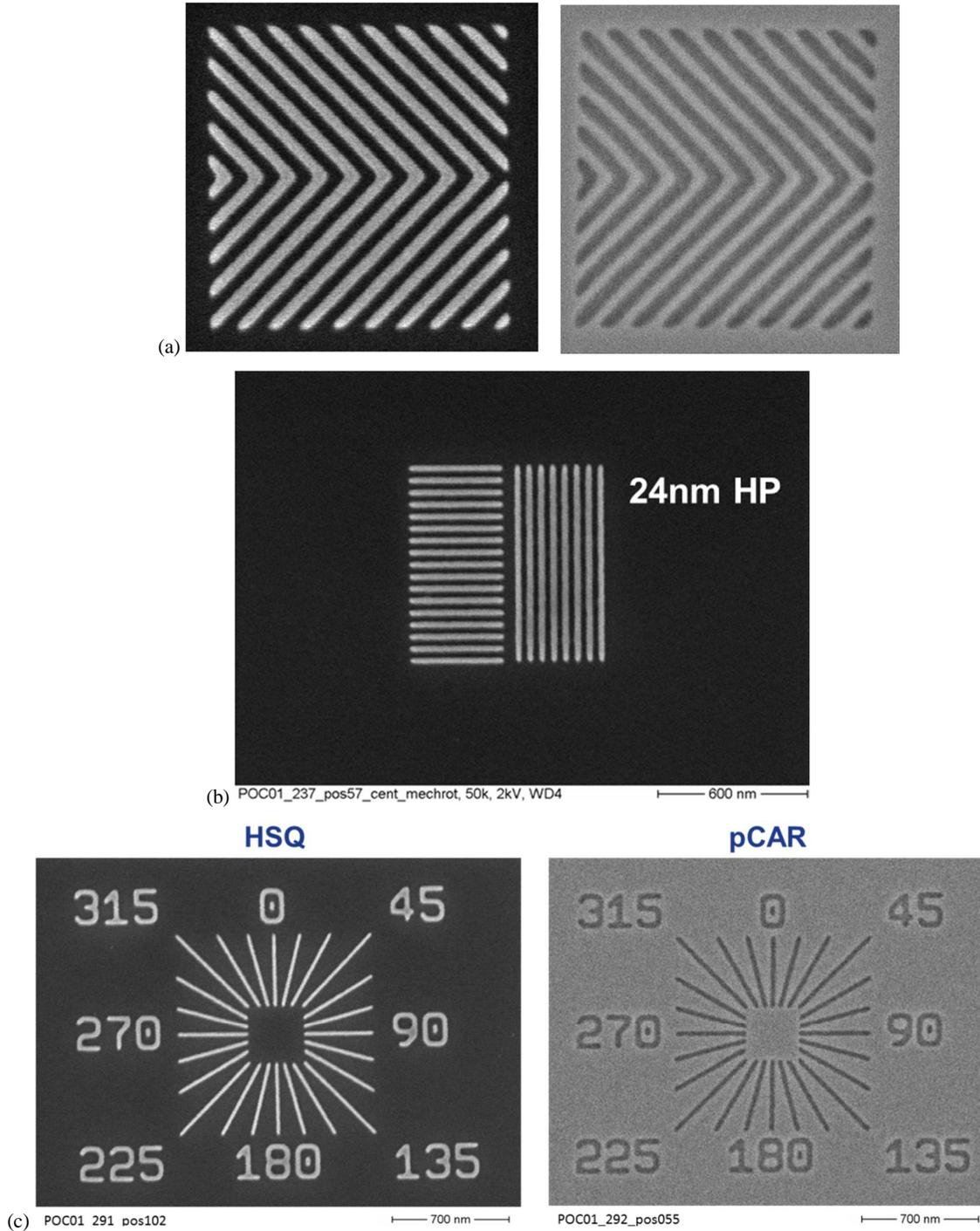
Figure 14: eMET POC resolution (a) 45° and 135° 30nm HP in HSQ negative (left) and pCAR positive resist (right), (b) vertical and horizontal 24nm HP in HSQ, (c) Any angle 24nm iso lines in HSQ and pCAR(numbers written with 30nm line width).

It is straightforward to change the beam size to e.g. 10nm by using an Aperture Plate (Fig. 4) with 2µm x 2µm openings. (For Beta and HVM tools there will be the possibility of in-situ change of beam size, as outlined in [xx]). Due to the small column blur (5nm 1sigma), the very small forward scattering of 50keV electrons in resist materials, and the small resist blur of e.g. insensitive pCAR resist, there is expectation that using 10nm beam size a resolution of 12nm HP can be achieved.

To achieve sub-10nm resolution there are possibilities to lower the aberration blur of the column optics with proprietary measures. Thus, as the chromatic / Coulomb interaction blur is very small, a total Column blur below 5nm 1sigma will become possible. To realize sub-10nm resolution a smaller beam size of 8nm or 5nm will be used.

6. eMET MULTI-BEAM MASK WRITER ROADMAP

There are stringent ITRS requirements to lower the 3sigma line width roughness (LWR) for future mask technology nodes. This can only be accomplished by enhancing the resist exposure dose to $50\mu C/cm^2$ - $100\mu C/cm^2$ for the 11nm HP mask technology node and below (Fig. 15).
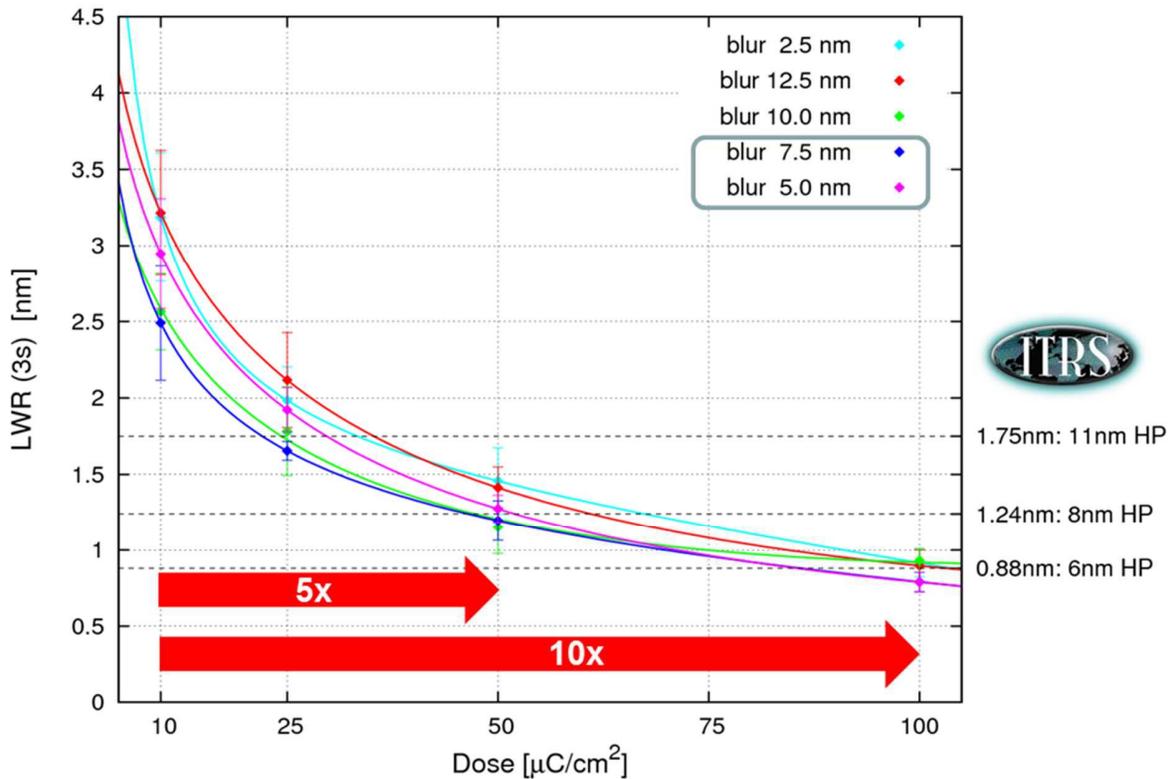

Figure 15: Monte Carlo simulation of the 3sigma line width roughness (LWR) for 30nm line width vs. resist exposure dose. Parameter is the combined tool and resist 1sigma blur. The optimum total 1sigma blur is between 5nm and 7.5nm, meeting the requirements for the 6nm HP mask technology node when using a resist exposure dose of $100\mu C/cm^2$.

The eMET roadmap for multi-beam mask writer (MBMW) tools is outlined in Figure 16. The realized multi-beam column is used for Alpha, Beta and 1st generation HVM (high volume manufacturing) mask writer tools, providing 256k (k=1024) programmable beams for MESA based multi-beam writing along 82µm wide stripes at constant stage velocity. The eMET Alpha Tool is realized 2014 integrating the column with a production worthy platform and stage. eMET Beta Tools are delivered in 2015 and first generation HVM Tools are scheduled in 2016.

	POC	ALPHA	BETA	1st gen. HVM
	2012	2014	2015	2016
Technology Node	Test: 11nm HP (8nm Logic)	11nm HP (8nm Logic)	11nm HP (8nm Logic)	11nm HP (8nm Logic)
Beam Array	82µm x 82µm	82µm x 82µm	82µm x 82µm	82µm x 82µm
# Beams (k=1024)	256k	256k	256k	256k
max Current (all beams "on")	1 µA	1 µA	1 µA	1 µA
Throughput ($\geq$ 100µC/cm²)	10 cm²/h	**15h/mask**	**10h/mask**	**<10h/mask**

Figure 16: eMET multi-beam mask writer (MBMW) roadmap

7. SUMMARY

eMET POC multi-beam writing is demonstrated with 24nm HP resolution and possibility to realize complex OPC and ILT mask patterns on 0.1nm address grid.

Using an insensitive pCAR positive resist, the resolution capability and throughput potential is verified for the 11nm HP technology node and below, where a resist exposure dose of 100µC/cm^2 is required.

First eMET MBMW Beta tools are scheduled for 2015, first HVM tools for 2016.

Productivity enhancements for 100WPH EBDW are possible, but remain a great challenge. To meet EBDW productivity, substantial investments in data path and system engineering are required.

REFERENCES

[1] Mahesh Chandramouli, Frank Abboud, Nathan Wilcox, Andrew Sowers, and Damon Cole, "Future Mask Writers Requirements for the Sub 10 nm Node Era", Proc. SPIE Vol. 8522, 85221K (2012)

[2] Sang Hee Lee, Jin Choi, Hee Bom Kim, Byung Gook Kim and Han-Ku Cho, "The requirements for the future e-beam mask writer; statistical analysis of pattern accuracy", Proc. SPIE Vol. 8166, 81661B (2011)

[3] Elmar Platzgummer, Christof Klein, and Hans Loeschner, "eMET POC: Realization of a proof-of-concept 50 keV electron multibeam Mask Exposure Tool", Proc. SPIE 8166, 816622 (2011)

[4] Yan Borodovsky, "EUV, EBDW – ArF Replacement or Extension", KLA-Tencor User Lithography Forum, Feb 21, 2010, San Jose, California, USA (2010)

[5] Hidetami Yaegashi, K. Oyama, S. Yamauchi, A. Hara, and S. Natori, "Sustainability of Double Patterning process for Lithographic scaling", SEMATECH 2011 International Symposium on Lithography Extensions, Oct 20-21, 2011, Miami, Florida, USA (2011)

[6] Mark Melliar-Smith, "The Future of Lithography – Back to Single Patterning? Or the Rise of DSA & Multiple Patterning?", Feb 26, 2013 Joint Panel at SPIE Advanced Lithography 2013, San Jose, California, USA (2013)

[7] Burn J. Lin, "Future of multiple-e-beam direct-write systems", J. Micro/Nanolith, MEMS MOEMS (JM3), 11(3), 0033011 (Jul-Sep 2012)

[8] Shusuke Yoshitake, Takashi Kamikubo, Noriaki Nakayamada, Kiyoshi Hattori, Hiroyushi Ando, Tomohiro Iijima, Kenji Ohtoshi, Kenichi Saito, Ryoichi Yoshikawa, Shuichi Tamamushi, Rikio Tomiyoshi, Hitoshi Higurashi, Yoshiaki Hattori, Seeichi Tsuchiya, Masayuki Katoh, Kouichi Suzuki, Yuichi Tachikawa, Munehiro Ogasawara, Victor Katsap, Steven Golladay, and Rodney Kendall, "EBM-8000: EB mask writer for product mask fabrication of 22-nm half-pitch generation and beyond", Proc. SPIE Vol. 8166, 81661D-1 (2011)

[9] David Lam, Dave Liu, Ted Prescop, "E-beam Direct Write (EBDW) as Complementary Lithography", SPIE Photomask Technology (BACUS 2010)

[10] Akio Yamada and Yoshihisa Ooae, "Cell Projection Use and Multi Column Approach For Throughput Enhancement of EBDW System", Proc. SPIE Vol. 7823, 78231H-1 (2010)

[11] Matthias Slodowski, Hans-Joachim Doering, Wolfgang Dorl, Ines A. Stolberg, "Multi Shaped Beam: Development Status and Update on Lithography Results", Proc. SPIE Vol. 7970, 79700$ (2011)

[12] Elmar Platzgummer, "Maskless Lithography and Nanopatterning with Electron and Ion Multi-Beam Projection", Proc. SPIE 7637, 763703 (2010)

[13] Regina Freed, Thomas Gutiotti, Jeff Sun, Anthony Cheung, Jason Yang, Mark McCord, Paul Petric, Allen Carroll, Upendra Ummethala, Layton Hale, John Hench, Shinichi Kojima, Walter Mieher, Chris F. Bevis, "Reflective electron-beam lithography performance for the 10 nm logic node", Proc. SPIE Vol. 8622, 86221J (2012)

[14] M.J. Wieland, H. Derks, H. Gupta, T. van de Peut, F.M. Postma, A.H.V. van Veen, Y. Zhang, "Throughput enhancement technique for MAPPER maskless lithography", Proc. SPIE Vol. 7637, 76371Z-1 (2010)

[15] Christof Klein, Hans Loeschner, and Elmar Platzgummer, "50-keV electron multibeam mask writer for the 11-nm HP node: first results of the proof-of-concept electron multibeam mask exposure tool", J. Micro/Nanolith. MEMS MOEMS 11(3), 031402 (Jul-Sep 2012)

[16] Elmar Platzgummer, Christof Klein, and Hans Loeschner, "Results of Proof-of-Concept 50keV electron multi-beam Mask Exposure Tool (eMET POC)", Proc. SPIE 8441, 8441-58 (2012)

[17] Elmar Platzgummer, Christof Klein, and Hans Loeschner, "Printing results of proof-of-concept 50keV electron multi-beam mask exposure tool (eMET POC)", Proc SPIE 8522, 8522-52 (2012)

[18] Naoya Hayashi, "Computational Lithography and Challenges for Mask Making", LithoVision 2012, Feb 12, 2012, San Jose, California, USA

[19] Naoya Hayashi, "NGL Mask Readiness", The ConFab 2012 Conference, June 3-6, 2012, Las Vegas, Nevada, USA