Research on the output common mode voltage suppression technology of PWM inverter

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ABSTRACT

PWM frequency converter is one of the important tools in modern industry, which plays an important role in solving the production and application problems. However, the high voltage common mode voltage generated by it has certain restrictions on the use of PWM frequency converter. Based on this, this paper proposes the research on the output common mode voltage suppression technology of PWM frequency converter. First, the SPWM modulation uses the equivalent signal to replace the sine wave signal, and then the common mode voltage generated by SPWM is analyzed for data, explain the causes of the common mode voltage from the theoretical data, clarify the characteristics of the PWM inverter, analyze the influencing factors of the common mode voltage, and design the suppression method according to the influencing factors. Finally, the feasibility and correctness of the suppression method are verified through simulation experiments. In order to provide a new idea and method for the related research of the output common mode voltage suppression technology of PWM inverter.

Keyword:SPWM;Sort average difference; Frequency converter; Common mode voltage

1. INTRODUCTION

PWM inverter is responsible for the conversion between AC and DC power, which can change the frequency and voltage of power supply [1]. With the development of modern industry, PWM inverter is more widely used, integrated technology more complex, more new problems and technical barriers, inverter common mode voltage, will cause heat loss in the motor chip, and make the motor copper wire because of the skin effect, more energy consumption is one of the significant problems [2]. If the common mode voltage generated by the frequency converter is consistent with the intrinsic vibration frequency of the motor components, mechanical resonance will also be caused, which will reduce the service effect and the service life of the component itself [3]. Currently, the analysis of the common mode voltage generation mechanism focuses on the Fourier decomposition, the influence of the inverter parameters and different adjustment methods on the common mode voltage [4]. At present, the analysis of the common mode voltage is not sufficient, and the impact of the frequency converter parameters should be deeply explored in [5] in terms of analysis and experimental verification. This paper is committed to exploring the suppression technology of the output common mode voltage of PWM frequency converter to reduce the common mode voltage and reduce the adverse effects caused by using PWM frequency converter. Power utilization and modulation algorithm are the core technology points of suppressing common mode voltage. In this paper analyzes the SPWM common mode voltage, obtains the factors affecting the common mode voltage, studies the influence of the parameters on the common mode voltage, and finally conducts the simulation experiment. The experimental results show that the inhibition method has high feasibility and correctness.

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2. SPWM MODULATION AND COMMON-MODE VOLTAGE RESOLUTION

2.1 SPWM modulate

Sinusoidal pulse width modulation is one of the important techniques in common mode voltage suppression. Using the principle of impulse equivalence, that is, when the pulse impulse of different shapes and sizes acts on the inertial system, if the integral in time is equal, the effect is considered to be the same. In this paper, the pulse signal of equal amplitude is used to replace the sine wave voltage signal. In the frequency conversion power supply system, the signal with the width equal to the carrier amplitude is obtained, and then the constant voltage frequency ratio control is realized by adjusting the pulse signal.SPWM control adopts the scale sampling method in digital control, the principle is similar to the natural sampling method, but it can better optimize the calculation pressure. By setting the rules of power off, the carrier sampling data is consistent, and artificially set as positive or negative peak, then the corresponding sine wave instantaneous value and pulse width can be obtained.According to the geometric relation of carrier and sinusoidal modulated wave, To achieve the goal of symmetrical the SPWM pulse waveform of the plus and negative half cycles of a modulated wave, Of the sinusoidal function and carrier in the DSP, By changing the pulse duty cycle, The sampling value is obtained directly from the algorithm formula, From the perspective of the SPWM waveform shape, The high level width and the low level width from the positive or negative over zero remain consistent, During the synchronous modulation, , The carrier frequency changes with the modulation wave frequency, When the modulation wave is low, The corresponding carrier frequency is also low, But the output harmonics will get larger, therefore, Low-frequency modulation should be avoided when modulation, The performance should be controlled by high-frequency modulation.

2.2 Common mode voltage analysis

In MATLAB, the frequency conversion power supply system model is built. The power supply system includes asynchronous motor, power supply, inverter and other equipment. Among them, the modulation party of the inverter is [6]composed of PWM frequency converter and delay module.The model parameters are set as follows: power output, voltage is 100V, modulation wave rate is 50Hz, carrier frequency is 5 kz, voltage utilization is 0.6, dead zone time is 5, the three-phase motor resistance is 10, and the equivalent inductor is 50. Using the STM8051F020 single-chip microcomputer to control the PWM output pulse signal, which is in charge of the switch of the inverter, so that the inverter output the pulse signal of unequal width and height, used to replace the sine wave AC voltage signal, and finally complete the requirements of frequency conversion of [7]. To verify the correctness of the model, you need to turn off the power, power only the DPS control panel, run the program and observe. If the PWM waveform pulse waveform appears, the trigger pulse works normally. The PWM waveform is shown in Figure 1.

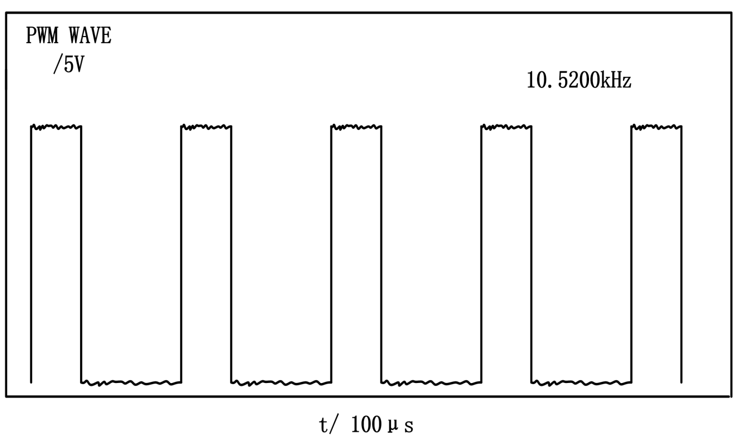

Figure 1. PWM oscillogram

In the figure, the vertical axis is the voltage and the frequency is 10.5200kHz. According to this test, the function of each model component is the same as the theoretical working principle. Through the test, the DC supply voltage can be obtained, and the carrier ratio and modulation method will have an impact on the common mode voltage.In the frequency conversion system, through the analysis of the inverter output to obtain the common mode voltage, the output waveform expression of the corresponding voltage should be calculated by the regular sampling algorithm, and the voltage of the other two phases is obtained through the phase transition, and finally the H voltage is superimposed。 Therefore, the modulation frequency wave is f_A , And the amplitude is U_A , The carrier frequency is f_B , And the amplitude is U_B , In the SPWM method, N is the ratio of carrier frequency and modulation wave frequency, expressed as formula (1):

$$N = f_B / f_A \tag{1}$$

The ratio of frequency modulation wave amplitude and carrier amplitude is the M modulation system ratio, which is expressed as (2):

$$M = U_A / U_B \tag{2}$$

In this, M affects the utilization of voltage, and the width of each pulse in SPWM wave is related to M and N one by one. Therefore, it can be seen that the common mode voltage resolved voltage utilization of SPWM is very important for the common mode voltage.

3. COMMON MODE VOLTAGE CALCULATION

3.1 Effect of PWM characteristic common mode voltage

It is pointed out in the previous theory that since SPWM waveform corresponds to the modulation wave pulse, the factor affecting the common mode voltage value is the key to suppress the common mode voltage. Through analysis, it can be known that the supply voltage, carrier ratio, modulation mode and dead area can all have an impact on the common mode voltage[8]. Regarding the common-mode voltage suppression of the dead-zone effect, Since the common mode voltage in the dead zone time is basically equal to the peak of the common mode voltage at the zero voltage, So it can effectively inhibit the peak of the common mode voltage, first, Need to measure the current direction, Due to the characteristics of the common mode voltage independent of the inverter switching state under the action of IMC zero current, Can realize the free switching of switches at the rectification level application, Because the feature is irrelevant, So in dead zone time, regardless of the switch status, Neither will have common mode voltage spikes due to vector switching, With the action of a vector, The common-mode voltage is determined by the bus-bar voltage amplitude, And the existing methods can suppress the voltage by 60%, However, when the IMC applies the zero-current vector, The voltage of the bus can be regarded as 0, There is almost no common mode voltage when the voltage is 0, Good results for suppressing the common-mode voltage.

3.2 Calculate the common-mode voltage affected by the PWM

The following analyzes the change of PWM from the supply voltage and the common mode voltage. According to the definition of the bus voltage, it is clear that the voltage utilization rate is related to the amplitude of the voltage base wave component. Therefore, the amplitude of the base wave component can be changed from the definition to change the utilization rate, so as to observe the influence of the utilization rate on the common mode voltage. The voltage is set to 100V, the dead zone time is 5 μ s, and the carrier frequency is 50Hz and the modulation wave frequency is 5 kHz. According to the common mode voltage and the influence result of the reaction rule, the calculated value is compared with the actual value, and the influence rule is summarized. The formula is (3):

$$V = U_1 / U_d \tag{3}$$

In the formula, U_1 is the amplitude of the fundamental wave component of the output voltage, U_d For the power supply voltage, the calculation formula of the power supply voltage amplitude is (4):

$$U_1 = (\sqrt{3} M U_d) / 2 \tag{4}$$

The change of the carrier frequency for the size of the common mode voltage is not big, repeatedly change the carrier frequency can find the carrier frequency increase, the effective value of the carrier frequency did not change significantly, and the carrier frequency attenuation, the effective value is not significantly changed, the components of the harmonic in the integer multiple of the frequency, thus, the change of the carrier frequency on the suppression of the common mode voltage [9]. SPWM modulation is proportional to M modulation, the power supply voltage is fixed with the dead zone time, when the utilization rate increases, the effective value of the common mode voltage is gradually reduced, and the effective value of the harmonic component at the carrier frequency is reduced along with the effective value of the common mode voltage, so the utilization rate plays an important role in the common mode voltage suppression [10].

4. CO-MODE VOLTAGE INHIBITION

4.1 Recent level approximation modulation

By understanding the characteristics, the nearest level approximation modulation in the sorting equalization algorithm can be modulated in the voltage suppression. This modulation can be realized by gradually approaching the sine wave to control the waveforms of different bridge arms. The level approximation along with the modulation graph is shown in Figure 2.

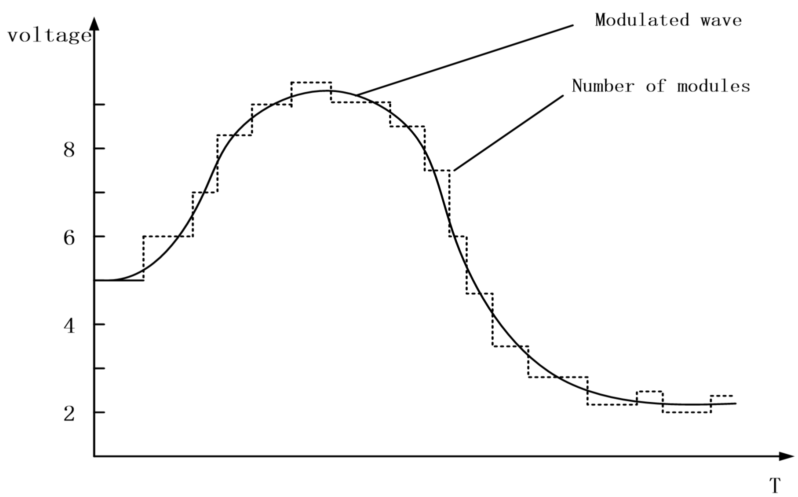

Figure 2. Level approximation modulation

As we can see from FIG. 2, when the voltage is higher, the more modules are used, and the number of modules is related to the waveform voltage in real time, and the number of modules is linearly represented as a zigzag shape.

If U1 is the reference value of modulation wave at phase i and U0 is the voltage at phase i, formula (5) (6):

$$N1 = N / 2 + round(U1,_i / U0) \tag{5}$$

$$N2 = N - N1 = N / 2 - round(U1,_i / U0) \tag{6}$$

In N1, N2 represent the modules on different bridge arms, where round (x) represents the nearest integer number to x, and a single bridge arm can contain N modules. If the modulation wave is increasing, the number of modules is also increasing, while if the modulation wave is weak, the number of modules will decrease.

At present, has learned the number of modules, but not all the time required for the same, can use sorting pressure algorithm for control, first of all, the module voltage sampling, minimum before the sort, second, determine the current sampling direction, finally, the current is regular charging, select voltage minimum module applied to the bridge arm, the current is negative means discharge, should choose the maximum voltage module applied to the bridge arm.Since the number of modules required to be applied to the bridge arm is obtained by the sorting and pressure equalization algorithm, rather than the signal corresponding to each module, the number of modules can be further processed before the module is applied to the bridge arm, so as to realize the theoretical suppression of the common mode voltage.

4.2 Six-segment partition voltage suppression

The suppression of the common mode voltage first needs to calculate the number of modules required by the bridge arm according to the nearest level modulation method, and then the six-segment modulation method is used to complete the suppression. The six-segment module planning diagram is shown in Figure 3.

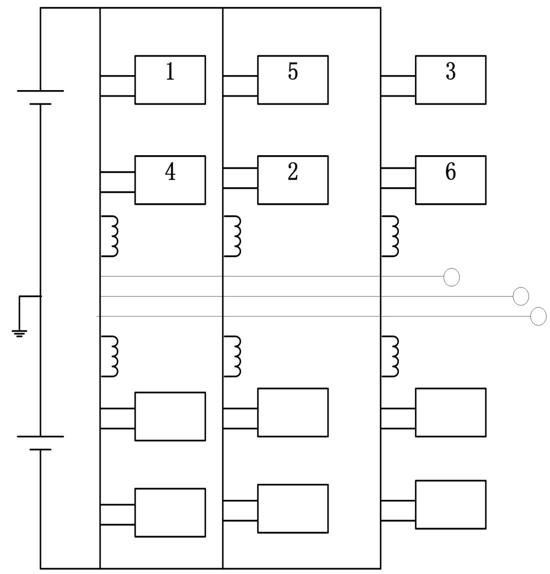

Figure 3. 6-paragraph module planning

According to FIG. 3, the six-segment scheme ensures that the carrier phase difference between two adjacent modules is not zero. In Figure 1,1 and 2 are located in diagonal positions, 1 is adjacent to 4 and 5, so that the sequence modules are not adjacent and the phase difference of exactly adjacent modules is equal. In the design, 60 is the section area, including U1 <U2 <U3, where U1,2,3 are the corresponding bridge arm voltage, and all the areas segmented in this way can be used as the control domain 1. First, a modulation wave, by calculating the required in the bridge arm the module number respectively A, B, C three pulse signal, then according to the size of the signal for the segment processing, according to the number of module needed to get new module number calculation rules, such as, calculation control section 1, calculate the bridge arm into module number use such as formula (7):

$$U_c = U_d / 6N(N_n - N_p) \tag{7}$$

In this, Uc refers to the common mode voltage, Ud is the DC input voltage, Nn is the total number of all modules available, and Np refers to the number of modules that do not meet the conditions. When Ud is determined, the difference before the module plays a role in determining the size of the common mode voltage. Take the three-phase bridge arm as an example, the k and N / 2 + k modules can be removed, and every six modules into a group, when the amplitude is determined, the size of the space vector and the arm Angle frequency positive correlation, so that the adjacent module corresponding to the carrier phase difference of 180, the first and the last phase difference of 180, ensure at least three switches working at the same time, and three switches are located in three different arms, after the module input can always maintain 3, equal to the number of modules after grouping, in order to suppress the common mode voltage.

5. CONTRAST EXPERIMENT

5.1 Experimental preparation

For the simulation experiments on the MATLAB simulation platform, The data information for the required design is as follows: bridge arm inductor 5 mH, Sub-module capacitor mF, Load resistance of 20, Load inductor of 1.25 mH, DC voltage: 800V, Carrier frequency is 10 kHz, An AC frequency of 50Hz, Modulation ratio of 0.95, For the actual used component data, according to the above calculation method, Calculate the corresponding numerical value, Spectative results of the experiment, And is used to compare it with the actual test data, To ensure the normal operation of the experiment, Current waveform observed by using PSC-CPS-SPWM modulation before the experiment, When it can work properly, The traditional method is compared with the current method。

5.2 Experimental result

According to the PWM waveform to judge whether the pulse is normal, the power supply is turned on and the voltage is gradually increased, and the asynchronous motor starts to work. Using the asynchronous motor data at the one end of the probe and the inverter data at the other end, the waveform state of the working mode voltage can be obtained. The results show that the shape of the common mode voltage is the same as the data calculated before the experiment, which verifies the correctness of the theoretical analysis and shows that the frequency converter can work normally. Then, the inhibition effect of the traditional method and the design method of the paper on the common mode voltage is tested respectively. The experimental results are shown as in Figure 4.

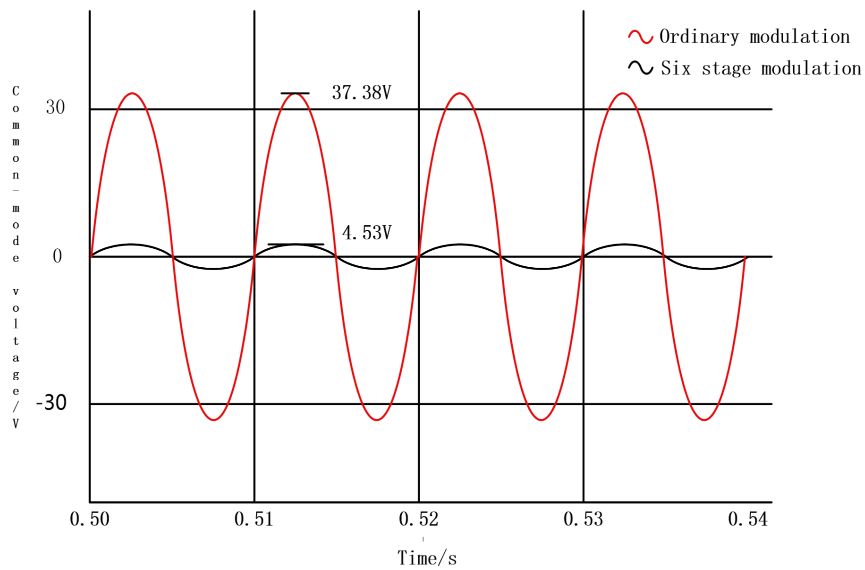

Figure 4. Experimental results compare

Judging from Figure 4, the red sine wave is the traditional common mode voltage suppression method, and the voltage peak is 37.38V. The black sine wave uses the six-segment module to plan that the peak voltage is 4.53V. Compared with the ordinary algorithm, the peak common mode voltage is suppressed by 82.5%. The reason that the voltage is not zero includes the fluctuation of the module capacitance voltage. The experimental results show that the common mode voltage.

6. CONCLUSION

In conclusion, this paper carries out the experimental verification on the bionic platform, the experiment shows that under certain constraints, using the algorithm to suppress the common mode voltage can achieve higher efficiency, lower loss, reduce the reliability of the output common mode voltage suppression technology of PWM inverter. This paper controls the utilization rate of the power supply voltage as the constraint condition, analyzes the causes of the common mode voltage, uses the nearest level approximation modulation mode, calculates the module planning strategy, and uses the six-mode optimization method to suppress the common mode voltage. After theoretical and experimental exploration, this paper obtains the way to reduce the common mode voltage. In the future research, we will continue to explore more effective suppression methods, and the voltage suppression technology is studied and discussed from a new perspective.。

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