Intel Nanotechnology Integrated Process Control Systems: An Overview

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ABSTRACT

As patterning dimensions decrease, die yield and performance become increasingly sensitive to smaller amounts of process variations. To minimize variability, Process Control is applied to prevent excursions, improve yield, decrease non-product runs, reduce cycle time due to rework, and reduce equipment calibration and maintenance. Intel inline Process Control aims at rapid detection, classification, prediction, and correction of problems and/or non-optimal performance during wafer processing. For efficient process control, robust analysis is needed in order to monitor the process, detect, and predict the process behavior. The paper will address Intel model based control and will focus on the various model based analysis and control modules that Intel has developed, and deployed for different technology generations. With the rapid increases in the number of analysis and control modules and the emerging need for integrating such modules to allow sharing of data, applications and methods, there is a need to define standard interfaces for such modules. This need motivated Intel to lead the development of SEMI E133; the Process Control Systems (PCS) Standard that was approved on October 2003.

1. INTRODUCTION

The ultimate goal of Process Control Systems (PCS) in manufacturing is to be able to predict, with increasing certainty as the product moves through the manufacturing line, what the functional characteristics of the device will be. Robust and efficient Process Control mechanism results in significant manufacturing cost reduction and reduces product variation. By definition [1-6], Process Control can be done through many capabilities or Functional Groups [3]. These include run-to-run (R2R) control, fault detection (FD), fault classification (FC), fault prediction (FP), and statistical process control (SPC).

Development and implementation of the optimal process control mechanism involve three phases [7-9]:

- Phase I: PCS monitor data from process, defect and metrology measurements to determine if the process equipment is performing in a consistent manner.
- Phase II: PCS are integrated together. At this point, knowledge exists on the link between process anomalies and the physical characteristics of the device. Also, either through the use of designed experiments or first principles modeling, it is known how to adjust various recipe parameters in order to minimize variation in the desired device characteristics.
- Phase III: Availability of models which not only link process equipment performance to device characteristics, but to ultimate performance characteristics.

To achieve the objectives of phase II and III, PCS will need sophisticated data publishing, analysis and mining capabilities which must be sensitive, robust and fast. Data analysis is crucial in identifying sources of variations and in recommending decisions. With the Nanotechnology introduction at Intel, data analysis is becoming more complicated, requiring more time for model development, testing and validation. In addition, models may be shared between different capabilities and applications. Current PCS applications are reasonably good at providing the requisite capabilities, but they are poor at working together. Limited data sharing, components interaction and model integration reduce IC makers' ability to aggressively reach Phases II and III objectives.

Data Analysis and Modeling for Process Control, edited by Kenneth W. Tobin, Jr., Proc. of SPIE
Vol. 5378 (SPIE, Bellingham, WA, 2004) · 0277-786X/04/$15 · doi: 10.1117/12.543298

The paper will first address the basic elements of a generic Process Control application with focus on the data analysis part. This will be followed by presenting two of Intel Analysis and Control modules for Critical Dimension (CD) and Overlay (Registration). Results will be shown for both modules to prove that accurate model based analysis is needed for precise and efficient Process Control. Finally, due to the fact that there is a lot of data sharing between the tools (process, metrology) and the applications (analysis and control) and between the applications themselves, there is a need for standard interfaces for process control applications. Intel role is leading the development of this PCS Standard SEMI E133 that was established last year will be outlined.

2. DATA MODELING FOR PROCESS CONTROL

Each PCS implementation has the following three basic elements [7-9],

- **Data Acquisition**: Wafer/lot, equipments/tool data are collected at one of the following phases of wafer processing:
    - ***During*** processing: *real time* (usually in-situ) data are collected and analyzed to ensure that tool/process is running within specs. For example, temperature and pressure measurements may be collected during wafer processing to ensure excursion free environment and alarm users in case of mis-processing [7]
    - ***After*** processing***:*** *Post process* data are collected to monitor the health of a process or a tool. As an example, Overlay and Critical Dimension measurements are collected from metro tools and analyzed to determine if material will be passed, re-processed or scrapped [4]. Control actions may be taken to adjust/stop tool or hold lots [5]
    - ***Before*** processing: measurements are collected, analyzed and analysis results are employed to adjust the tool *before* next wafer, lot or batch is processed. Example: analyzing metro data and feeding adjustments to tools before lots are processed [5]
- **Data Analysis**: Computational methods, algorithms, empirical relations, and statistical techniques may be applied on the collected data, resulting in a reduced set of data points that enable decisions making and actions taking [1], [2], [4].
- **Decisions and actions**: Based on analysis results, decisions can be made and actions may be triggered (if needed). Decisions may be wafer, lot, batch, or tool/equipment based [6-8]. Decisions may include material disposition (pass, fail or rework), tool shutdown, lot holding, and/or user notification. Also, based on analysis results, control actions may be invoked to adjust tool or change recipe.

As can be seen, all PCS implementations handle data in a consistent way (collection, analysis, decisions and actions). That consistency leads to the introduction of the PCS Analysis Engine (AE) concept [3], [7]. Using this concept, any PCS functional group (SPC, R2R, FD, FC, and FP) can be modeled as an AE with inputs representing measured and configuration data, and outputs representing results, decisions and actions [3]. The conceptual PCS AE was the first driver of the integrated PCS Framework at Intel [9], [13].

To achieve the desired levels of process control and minimize variations, each AE will employ a specific type of data modeling. Accurate data modeling mechanisms are needed to analyze and predict the system behavior. Data modeling mechanisms should take into account all factors and parameters that introduce variability. Among them, changing operating conditions, process unknown disturbances (for example: tool characteristics, specs change with time), process drift, and nonlinearity included.

Data modeling and analysis features include the following:

- Timing: Covers the time window for analysis execution (before, during or after processing)
- Disposition: Indicates if disposition and decisions will be wafer, lot or batch based
- Trend: Shows entity variation or change over time, or tool
- Smoothing: Applies data smoothing algorithms and techniques to collected measurements before analysis to reduce noise effects, outliers and measurement errors
- Offline analysis: Implies inline analysis methods, algorithms, and codes availability for offline systems/applications.

As can bee seen in **Figure 1**, each Process Control module is preceded by an analysis module. The process analysis module applies models (statistical, physical, empirical, or mixed) to the input data, and generates a few numbers/metrics. These numbers/metrics are fed to the control module which may employ other models to detect anomalies, monitor the process, and identify issues or out of control conditions and take actions if needed.

3. EXAMPLES OF INTEL DATA MODELING AND PROCESS CONTROL SYSTEMS

The section will address two examples that illustrate the utilization of data analysis and process control modules. We will focus on two Photolithography applications; CD and Overlay modeling and control. As can be seen in [14], patterning dimensions are shrinking and as a result, robust control is required to ensure the success of the patterning process. This translates to tighter control limits on both CD and overlay. With that robust control becoming a requirement, an accurate analysis module taking into account all sources of variation should precede the Process Control Module.

3.1 CD Modeling and Control:

Patterning variations can come from lithographic scanners or resist tracks and from etchers. Lithographic scanners can cause focus drifts generated by wrong focus offset in the scanner recipe and field level tilts causing substantial focus differences. Focus deviations result in changes in feature profiles and actual CDs. A CD modeling methodology was developed to take the CD data as inputs, fit a model and extract the systemic components that will be utilized to predict the CD levels at each point within the wafer. Finally, predicted CD's are summarized per wafer and/or per lot, yielding a smaller set of numbers that enable decision making and action taking.

The CD modeling results are shown in **Figures 2-5.** Here is a description of each one:

- **Figure 2**: The model predicts CD's at all points within the wafer and identifies locations with maximum and minimum CD's. The wafer CD's are then rolled up to the lot level and are reported to the SPC system. As can be seen, the maximum and minimum CD's are centered reasonably around the process target line.
- **Figure 3**: The CD range (which is the difference between maximum and minimum CD) is computed and utilized to identify discrepant lots so that engineers can track these lots and identify problems' root cause. As shown, three lots seem to have a higher range. That conclusion was supported by the E-Test results at the end of manufacturing line.
- **Figure 4**: Analysis module predicts CD's at all wafer locations to construct a CD wafer map. As seen, CD changes gradually from one side of the wafer to the other side. That represents a wafer tilt at towards the 10 O'clock direction.
- **Figure 5**: In this example, CD values are off target in most locations. That indicated an issue with the stepper and lot was reworked.

In summary, the analysis module results will enable taking the right decision for material disposition, and performing robust control by adjusting the tool settings (knobs) so that the process target and specifications can be achieved. The model was applied to predict the systemic components that cause the CD variation [16]. The R2R control module applies other models to compute and execute the necessary adjustments by changing the focus and exposure dose to get the desired levels of CD's. Results and improvements are summarized in the following table:

Partition	Diff Mean (%)	Diff SD (%)	Diff Cpk (%)
A	-0.4	-44.5	69.2
B	0.12	-56.3	128.7

This table displays the results of the EFCC (Exposure & Focus CD Control) module [16]. As can be seen, two data partitions A and B are considered. Each one represents a specific layer and a stepper. The relative difference in the mean, Standard Deviation (SD) and Cpk are computed before and after tool adjustments. Looking at the mean (target) difference, the EFCC control did not introduce any change to the mean. For the SD, there is a significant improvement (~44.5 % and ~56.3 %) when the control module was invoked. Moreover, the process Cpk improved significantly. In conclusion, applying the model based analysis to the control module led to significant improvements in the CD Standard Deviation, Process Cpk and kept the mean almost unchanged.

3.2 Registration (Overlay) Analysis and Control:

As known, yield and performance are dependent on the misalignment between layers (Overlay or Registration error). Therefore, it is important to develop a model that is capable of analyzing overlay. At, Intel, such a model was developed, taking registration data as input, performing the necessary calculations and yielding a set of systemic components utilized to predict the registration. Based on the predicted registration, the probability of die/wafer/lot failure is computed and pass/fail/rework decisions can be made. Moreover, the model can capture process drifts, which can be fixed using the R2R control.

The results of the registration analysis for different technologies are shown in **Figure 6**. As can be seen, the probability of failure is computed as a function of the specified tolerance which represents the allowed overlay budget for a layer. As the tolerance increases, the failure potential decreases and as a result, the associated probability of failure goes down. Although Intel has this analysis module running in its Fabs for years, every technology generation requires revising this module to enhance its accuracy and add new systemic components introduced by the newer technology. This graph shows that model 1 which represents an older technology has higher probability of failure compared to model 2 and 3 that were developed for newer technologies. This means that, due to the large overlay budget associated with older technologies, models were simple and used to over predict registration. As an example, at 60 nm threshold (overlay tolerance), **Figure 6** indicates that model 1 and 2 will result in significantly higher probability of failure which will lead to a wrong decision and definitely an erroneous R2R adjustment.

Looking at **Figure 6**, we can see several challenges associated with the continuous shrinking of patterning dimensions (Moore's law). To overcome this problem, accurate process modeling is needed and tighter control methods will be required for future technologies. Also, stepper precision in patterning layers should improve so that the overlay can be reduced. Accurate, precise, sensitive and reliable computational models should be developed to reduce both alpha and beta risks in the decisions made.

The results of model 3 were fed to an R2R control module which performed an automated adjustment to the stepper and the mean and standard deviation of the registration were recorded [15]. For an ideal situation, the mean and the standard deviation of the registration should be zero. The following table proves that applying the R2R control to adjust the stepper led to an improvement in the mean, standard deviation and the process Cpk. As shown in that table, two data partitions C and D were considered and results were compared to after the stepper registration control (SRC) was invoked to adjust the process based on the results generated by the analysis module.

Partition	Diff Mean (%)	Diff SD (%)	Diff Cpk (%)
C	-11.1	-2.6	25.0
D	-2.3	-14.5	14.2

4. PCS STANDARDS

Having a standard way of providing data from the process equipment to the data analysis and process control applications and then communicating results eases development for both the IC maker and the application developer. This will provide benefit to all parties and reduce both the development and implementation costs. In addition, achieving the PCS goals will require effective internal and external integration of different PCS applications. Also, having many analysis and control modules inside and outside the tool and the need to communicate between these modules to achieve the robust control require IC makers, tool suppliers and PCS software supplier to conform to a PCS industry standard [3], [11], [12]. This standard (if adopted) will allow Integrated Circuit makers and suppliers to focus on improved capabilities rather than customized integration, and decreasing the risk introduced with integrating new applications into an existing factory.

Intel took the initiative and created with SEMI the PCS SEMI Task Force in 2002. The task force goal was *"to define inline PCS architecture interfaces for run-to-run (R2R), fault detection and classification (FDC) and statistical process control (SPC) capabilities."* The Task Force developed the standards and on October, 2003, the PCS Standards ballot was approved and was given the E133 number. The benefits of such a standard would be reduced systems integration time and cost, and an acceleration of industry adoption of PCS technology. Manufacturing software suppliers (commercial or in-house) would use these standards to implement well-defined external interfaces to their process control applications. This will enable customers to integrate these systems more cost–effectively with one another and with other software systems required by the wafer fabrication process.

5. Conclusions

With the introduction of silicon nanotechnology, feature sizes are shrinking and as a result, smaller variations will adversely affect yield, increase non-product runs, rework, and equipment calibration and maintenance. Aimed at minimizing variability, PCS implementations/applications need to accurately detect, predict and correct anomalies to achieve the desired levels of process control. That will require precise and efficient data modeling to enable robust control which will lead to substantial gains in die performance, yield and fab output. In addition, PCS need to be integrated together to allow commonality leveraging, sharing data and components. To facilitate data sharing between tools, applications, and to enable PCS internal and external integration, Intel led the development of the PCS Standards SEMI E133 that was approved on October, 2003.

Acknowledgement

The authors would like to thank Dr. Joel Fenner, Dr. Cagdas Akturan, Dr. Hazem Hajj and Mrs. Cindy Morrison for their help in preparing this paper.

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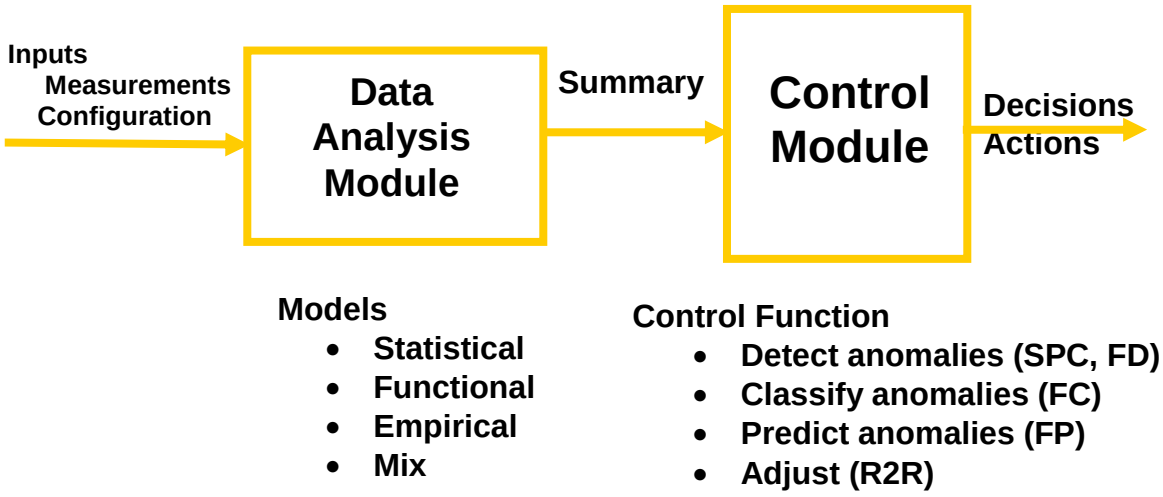

Figure 1: Functional Components of a PCS System

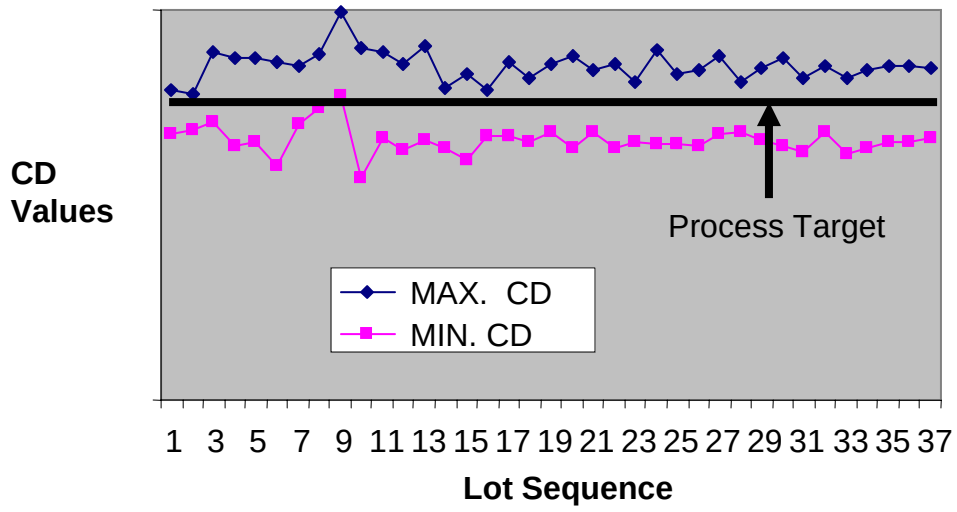

Figure 2: Predicted Maximum and Minimum CD across different lots

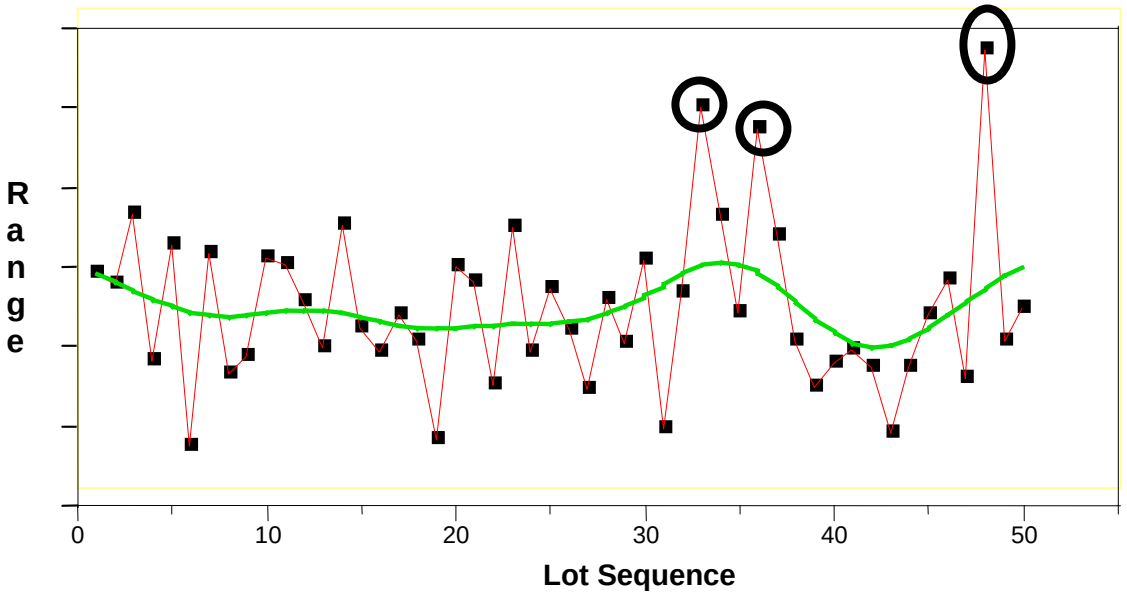

Figure 3: Predicted CD Range across lots to identify high range ones

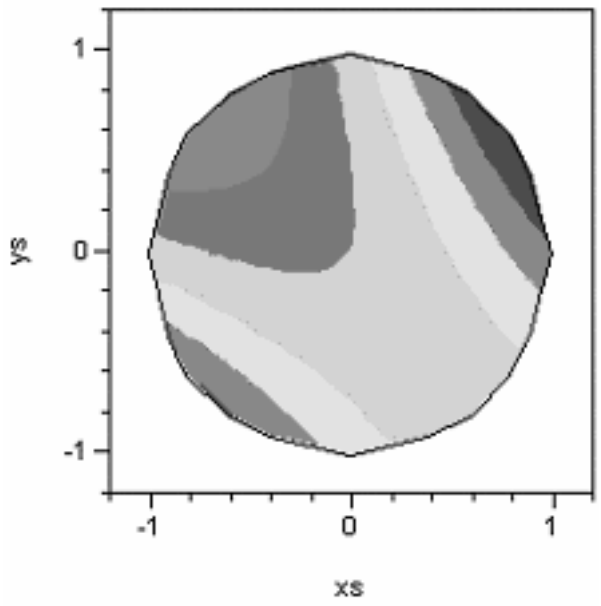

Figure 4: Predicted CD Wafer Map for a production wafer

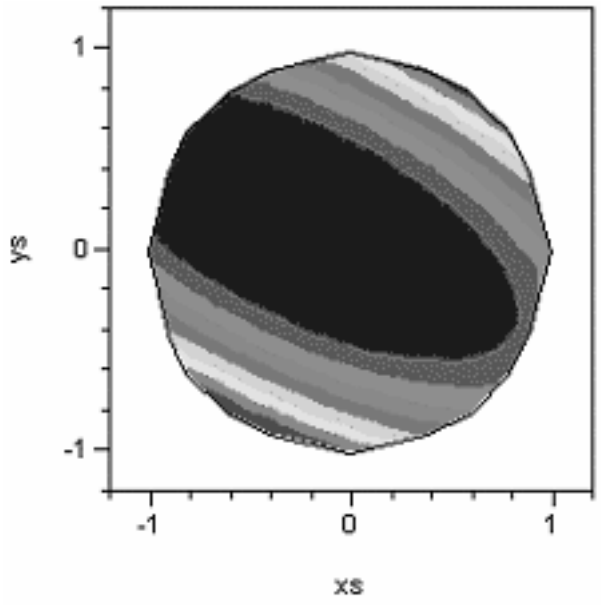

Figure 5: Predicted CD Wafer Map for a production wafer

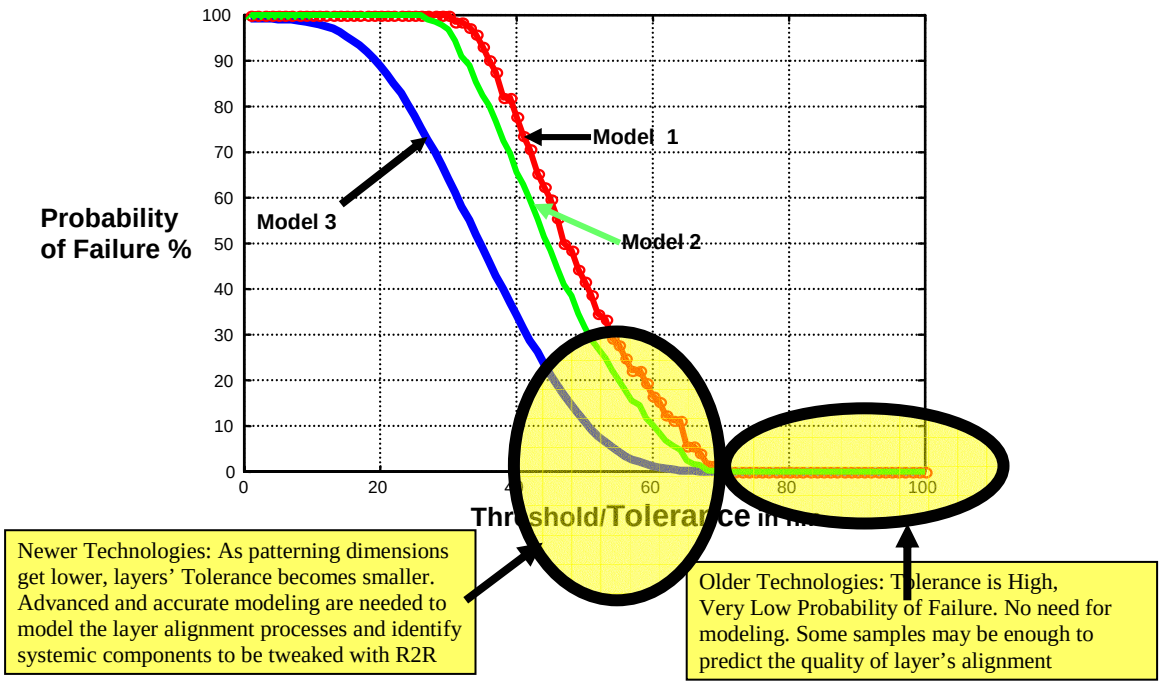

Figure 6: Probability of Failure as a function of the layer Threshold (tolerance). Models for three technologies were compared