Nanoimprint Lithography for Semiconductor Devices and Future Patterning Innovation

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ABSTRACT

Nanoimprint lithography (NIL) has been expected as a low cost lithography solution as well as pattern shrinking capability with superior Critical Dimension (CD) uniformity for several years. However, NIL had been considered having difficulty to be established as mass-production technology, unless the challenge of defectivity control is overcome. The defects of NIL are classified into the non-fill defect, the template defect, and the plug defect. In order to reduce these defects, establishment of the technical infrastructures is important with the innovations of equipment, material, and template technologies. Recently, the investment to lithography becomes heavier burden for a semiconductor device maker, as lithography technology has been more difficult for further pattern shrinking. Therefore, expectation of NIL realization has emerged again. This paper describes current NIL technical status and refers to a future NIL patterning innovation such as a desktop lithography.

Keywords: Nanoimprint, Lithography, Template, Defect control, Overlay accuracy, CD uniformity, Lithography investment

1. INTRODUCTION

There is no limit to the demand of human beings for memory capacity, and memory device price down has been kept required. Pattern shrinking is a strategy for memory device in order to carry out for the reduction of the cost per byte as well as multi quantum technology and 3D type memories. The demand of pattern shrinking for lithography will continue in future.

As shown in Figure 1, the extendable ArF immersion technology, for example spacer process double patterning will be one of choices for half pitch 30nm (hp30nm) node and beyond. However, the extendable ArF immersion technology process is very expensive and will be difficult for finer technology than hp20nm node due to optical limit. Therefore, next generation technology evaluations will be lead by high Numerical Aperture (NA) Extreme Ultraviolet Lithography (EUVL) and Nanoimprint as innovative lithography. Next generation technology will be determined not only by technical innovations but also by economical efficiency. This is because the purpose of our technical development is to realize the low cost process.

The high NA EUVL can be a candidate of the next lithography to be capable of finer technology than hp20nm. In addition, the further pattern shrinking is possible with the high NA EUVL and EUVL extendable technology. However, there are big challenges to EUVL realization like optical source power, mask infrastructure and resist performance. The light source maker's development road map is shown clearly about light source output performance improvement, and it is expected that the further development for the improvement will proceed as planned based on the requirement. EUVL resist performance requirements are not only sensitivity, Line Width Roughness (LWR), and resolution but also defectively for mass production. EUVL single exposure or double patterning technology will be selected for hp20nm and beyond depending on the resist performances.

It had been demonstrated that NIL has finer resolution capability with excellent CD uniformity and LWR as a low cost lithography technology. NIL is a simple technology and is capable to form critical patterns easily. On the other hand, its defectivity control is difficult, since the printing magnification between template and wafer is 1 to 1. Moreover, there are unique defectivity types which are peculiar to NIL process. Authors describe current NIL technical performances for semiconductor device fabrication, especially with a discussion about the mass production from defectivity control point of view. It is also discussed about a future NIL patterning innovation such as a desktop lithography.

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2. NIL IN SEMICONDUCTOR

2.1 Exposure Tool

The Jet and Flush Imprint Lithography (J-FIL) process is shown schematically in Figure 2[1]. The process starts with a template made from a standard 6025 photomask blank, and then the patterns will be etched into the glass using the same technology for phase shift mask fabrication. An array of pico-liter sized drops of a low viscosity imprint resist is spread across the field being imprinted as the template lowered onto the drops. When the surface tension of the liquid phase imprint resist has been broken, capillary action draws the resist into the template features. Once filling is complete, ultraviolet (UV) light, passing through the glass template, is used to cross link the resist and convert it to a solid. The template can then be withdrawn and the process repeated on the next field. The J-FIL tool made from Molecular Imprints, Inc. (MII) is suitable as NIL equipment for semiconductor lithography from the following three reasons.

1. A template and a wafer are non-contact by using low viscosity UV curable imprint resist.
2. Dispense drops are arranged depending on the layout of a pattern density.
3. Intra-field overlay error can be compensated by tool.

One of NIL's strengths is a CD uniformity (CDU) performance. NIL patterning is direct pattern formation from template to wafer without development. Current Electron Beam (EB) writer's CDU on template is around 1 nm (3sigma), then NIL patterning on wafer is expected to be possible to make patterns with around 1nm (3signa) CDU. Figure3 shows CDU result of hp28nm dens pattern imprinted by MII tool. 1.2nm (3sigma) of CDU is obtained by 240 measurement sites (12 sites/shot and 20 shots/wafer).

Generally, NIL is considered to have a weakness with overlay accuracy performance. However, NIL has no projection lenses, and thus overlay accuracy cannot be influenced by the distortion caused by the aberration of lens system. The patterning magnification from NIL template onto the wafer is 1 to 1. Considering NIL total overlay contributors analysis, almost of all errors are from template EB writer distortion called registration. On the other hand, current EB writer registration is improving for around 5nm (3sigma) or better. Moreover, MII tool has intra-field overlay error compensation system. Figure 4[2-3] shows an experimental result of MII NIL tool overlay accuracy. Authors had obtained 10nm overlay accuracy by MII NIL tool. As EB writer registration will be improved, it is expected that NIL overlay accuracy will also be improved further.

2.2 Template

Imprint lithography uses templates made with commercial photomask materials and processes. For higher resolution applications, imprint templates can be written with variants of EB direct write tools, usually Gaussian Beam systems with 100keV of acceleration voltage. These tools have unparalleled resolution, and can easily produce templates with resolved dimensions of down to around 14nm. It can also provide an imprint resolution capability with excellent CDU beyond the possible performance with existing optical technologies, as shown in Figure 5[4]. Using commercially available Variable Shape Beam (VSB) mask writers with 50keV, imprint templates are already being written down to hp22nm dens line and space patterns and hp26nm contact hole patterns with very high quality of feature fidelity. Although process development engineers are occasionally compelling the resolution performance to be capable down to below 20nm, it is not the only issue for EB mask writer. As described above in the previous section, registration performance is important as it directly affects the overlay performance. Recent progression of registration performance is notable driven by the requirement from double patterning technology. For overall template fabrication technology point of view, the defectivity improvement is important and this topic is discussed in the next paragraph in detail. Further improvement of NIL template technology especially for resolution performance to achieve hp20nm and beyond will depend on the performance of EB resist processing.

2.3 Advanced device applications by NIL

NIL is convenient to be applied advanced device evaluation very easy and the cost is much less expensive. The example which performed gate integrity of memory device characteristic evaluation using NIL is shown in Figure 6. This test is evaluation of capacitance characteristic degradation as a function of gate width. NIL patterning was applied 3 layers with alignment between layers for test device fabrication. In this process evaluation, characteristic degradation of capacitance is observed by 28nm or less dimensions. From this example, it is effective in research and development of an R&D level especially, since NIL can perform leading edge device evaluation easily. Figure 7 shows an electrical open circuit yield test result for simple metal layer of device by NIL patterning. This test device was arranged with many electrical circuits that include several dimensions of the pitch, and several circuit length patterns. If a part of circuit is disconnected, electric current does not flow into a circuit. We obtained the yield with hp28nm by NIL technology from this result. However, we could not obtain the yield on the long circuit length. This result indicates that NIL still has a challenge to improve the defectivity.

3. SUBJECT AND VISION TOWARDS NIL MASS-PRODUCTION APPLICATION

3.1 Classification of NIL defects

The defects can be originated by imprint process and also from the template. Reduction of the imprinting defects needs the improvement of imprint system and imprint resist performance. For the template defect reduction, it is initially expected to have the progress of defect inspection technology. The inspection equipment technology needs the full area inspection at high speed by die-to-database inspection using EB technology. NIL is effective in only test device evaluation development, unless the technology of defectivity reduction is realized; device mass-production application is not easy. Figure 8 shows classification of NIL defects into the non-fill defect caused by bubbles in resist, the template defect, and the plug defect. In order to reduce these defects, it is important to establish the infrastructures along with the technical innovations of equipment, material, and template.

3.2 Non-fill defect

The non-fill defect is generated when a template approaches a wafer. The residual bubbles in resist will not form patterns. The residual bubble defect is called non-fill defect. In order to reduce the non-fill defects, it is very important to develop the method for quick dissipation of residual bubbles from the ambient between a template and a wafer, including new material of imprint resist development.

3.3 Template defect

It can be expected that template defects performance, as supplied by the commercial photomask vendors, can typically be less than $1cm^{-2}$. The optical mask defect inspection system, NFT6000 is assumed to be capable for the template down to around hp20nm node. However, for further finer node below hp20nm, optical method will not have a sufficient inspection for defectivity and EB mask defect inspection will become to play a key role for template defect inspection. The major challenge of this is to extend the life of the templates by the time they need to be removed from the imprint tool and re-cleaned. Template infrastructure has not been established yet for the related areas such as EB writer, defect inspection, development, cleaning, and repairing technology.

3.4 Plug defect

The plug defect is generated by tearing out of imprint resist when a template is separated from patterns on a wafer. In order to reduce plug defect, it may be required the new imprint resist material which, for example, has higher mechanical strength.

The other idea is to control the lubricous performance from “tribology” consideration on the surface of a template. Authors developed a NIL desktop lithography system called “PETAN#1” to study tribology of the template surface characteristics and it is described in Figure 9[5]. PETAN#1 consists of wafer chuck, template stage, a manual UV light and weight gage when a template is separated from a wafer. Imprint resist material is dispensed on a wafer, and template stage is rotated when a template approaches a wafer. The UV light is illuminated on the wafer passing through the template. The adhesion force is measured by weight gage when the template is separated from a wafer after imprint resist is hardened by UV light. The PETAN#1 was fabricated as NIL proto tool for desktop lithography. PETAN#1 was designed with the dimensions of 300mm X 300mm X 250mm, weight of 12kg, and its template size of 70mm X 70mm. PETAN#1 can form critical patterns simply at a low cost.

Authors prepared several processes to apply to template surface with Chemical Vapor Deposition (CVD) to identify the best performance material with minimum frictional force which contributes to have low adhesion force between template and imprint resist as described in Figure 10. The adhesion force by separation was measured by PETAN#1 for templates with several materials on surface. Figure 11 shows an experimental result of a measured adhesion force to several surface materials on template. B process has the minimum adhesion force among these processes, and is better than quartz (Qz) template. Authors are now studying to make a good process to reduce plug defects by applying new materials on template surface.

4. CONCLUSION

What is the main purpose of lithography technology innovation? Needless to say, it is the profits creation in semiconductor manufacturing. Pattern shrinking technology, productivity innovation for investment cost reduction, device yield improvement, etc. have been advancing for the means of this purpose achievement now and future. Especially pattern shrinking is not the purpose but the means of profits creation. If the pattern shrinking technology is not connected with profits creation, it is like putting the cart before the horse. The purpose of selection of a lithography method is in the profits creation which aims the improvement in device performance, and cost reduction for

semiconductor device makers. The lithography technology has been evolved and screened for about 30 years. From now on, the lithography and patterning technologies will continue to be evolving for ever adapting to circumstances of a device structure, a process improvement, business environment, etc.

In the NIL field of these days, new patterning technology proposals such as roll to roll imprint[6] is presented. NIL is existing technology in which not only semiconductor but also solar cell, Light Emission Diode (LED) and Hard Disk Drive (HDD) Patterned Media (PM) are potential markets as next-generation patterning technology. The large amount investment in advanced research development results in a large burden for a company. In the research and development environment, a huge clean room is not required. The advanced processing technology development demands technology with less expensive, simple and small like desktop lithography. The technical development which disregards economical efficiency for the enterprise is meaningless. We have to concentrate the wisdom in the world and realize the next generation patterning revolution.

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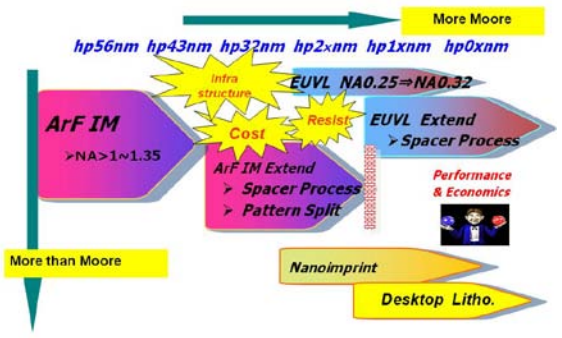


Figure 1. Lithography Roadmap

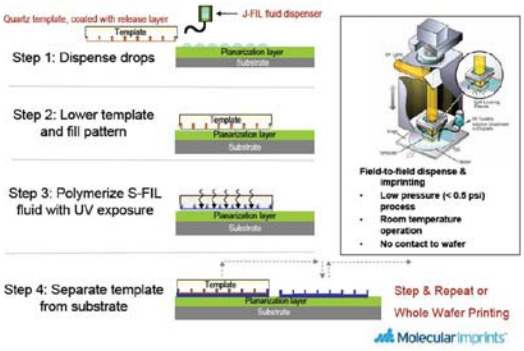


Figure 2. Schematic of the SFIL-O process.

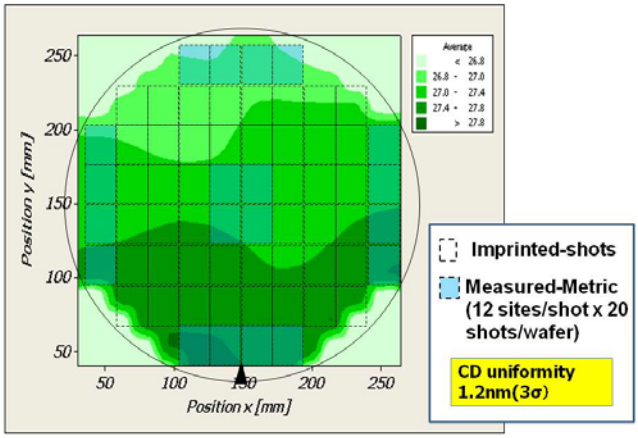
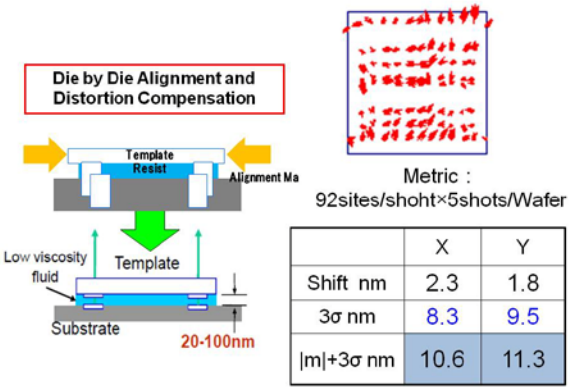


Figure 3. CD uniformity of hp28nm dense pattern



	X	Y
Shift nm	2.3	1.8
3σ nm	8.3	9.5
|m|+3σ nm	10.6	11.3

Figure 4. NIL Overlay accuracy result

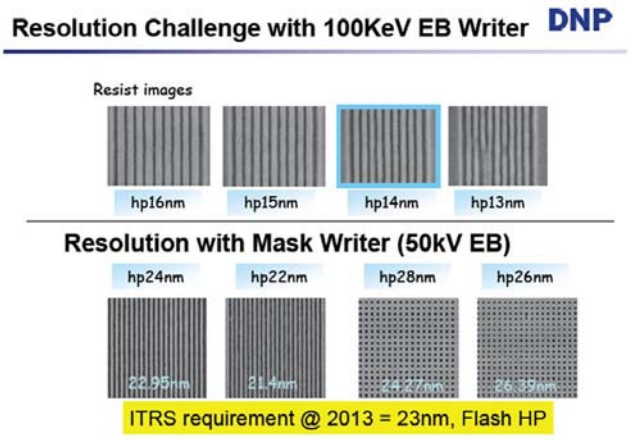


Figure 5. Resolution performance of NIL

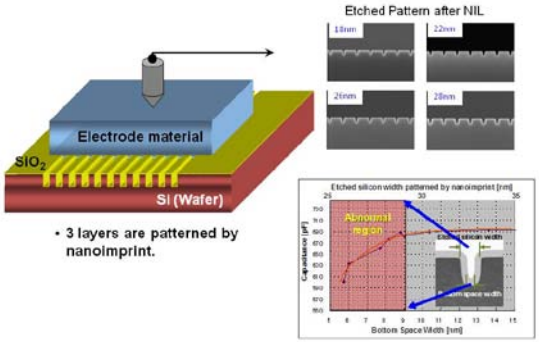


Figure 6. NIL device application for gate performance

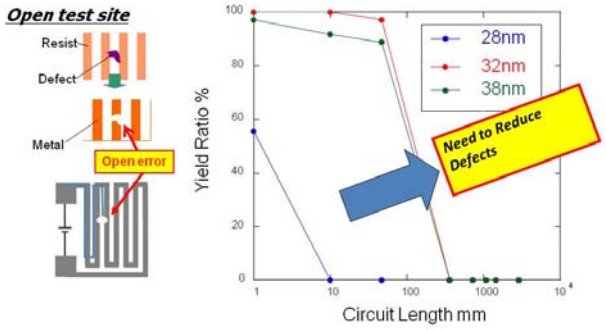


Figure 7. NIL electrical open circuit yield test

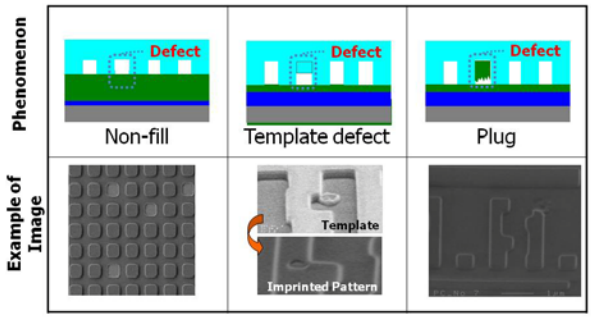


Figure 8. Classification of NIL defects

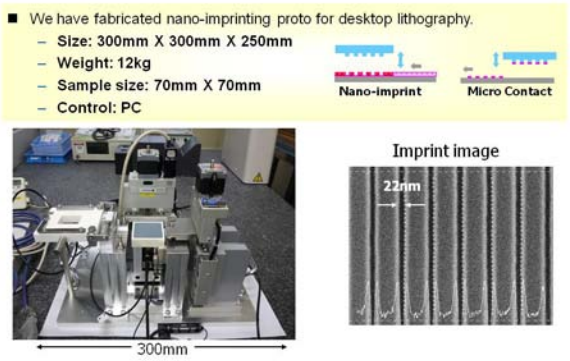


Figure9. NIL desktop lithography system

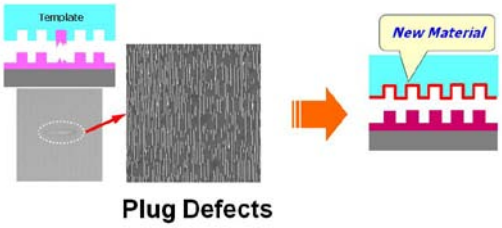


Figure10. Reduction of plug defects

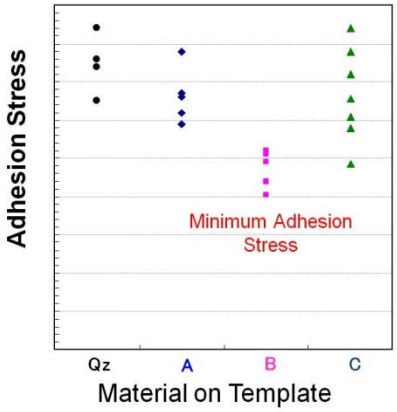


Figure11. Adhesion stress to template surface materials