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SEDHI: DEVELOPMENT STATUS OF THE PLÉIADES DETECTION ELECTRONICS

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ABSTRACT

In the framework of the Pléiades program, Alcatel Space is developping with CNES a new concept of Highly Integrated Detection Electronic Subsystem (SEDHI) which lead to very high gains in term of camera mass, volume and power consumption. This paper presents the design of this new concept and summarizes its main performances.
The electrical, mechanical and thermal aspects of the SEDHI concept are described, including the basic technologies: panchromatic detector, multispectral detector, butting technology, ASIC for phase shift of detector clocks, ASIC for video processing, ASIC for phase trimming, hybrids, video modules... This concept and these technologies can be adapted to a large scale of missions and instruments. Design, performance and budgets of the subsystem are given for the Pléiades mission for which the SEDHI concept has been selected.
The detailed performances of each critical component are provided, focusing on the most critical performances which have been obtained at this level of the Pléiades development.

1. INTRODUCTION

In the framework of studies relative to future earth observation optical systems, Alcatel Space has proposed to CNES a new concept of Highly Integrated Detection Electronics Subsystem (SEDHI).
This architecture may be summarized by the following characteristics:

- video processing entirely integrated on the focal plane
- high speed digital link
- digital processing in dedicated units in the satellite.

The possible architectures for the detection electronics and the associated selection process have been discussed in references 1 and 2. In the architecture selected for SEDHI, the complete video processing is included in the focal plane proximity electronics. This highly integrated concept optimizes instrument radiometric performances and interface budgets (mass, volume, power consumption), and will allow to take into account the new generation requirements of increasing frequencies, number of video chains, large dimensions focal planes with multiple spectral bands, which is the case of the Pléiades program. The assembly integration and test operations will also be simplified by the limitation of electronic units. Thus, the SEDHI concept may be summarized by : radiometric performance optimization at lowest costs.

The following paragraphs give a technical description of the main elements of the SEDHI which has been selected for the Pléiades instrument, summarize the main performances which have been measured at component and sub-system levels, and provide the budget for the complete detection subsystem.

2. FOCAL PLANE DESIGN

The Pléiades focal plane is shown on the next figure. The size of the focal plane is close to 400 mm and is analyzed in 30,000 samples in PAN (PANchromatic) and 7,500 in XS (Multispectral).

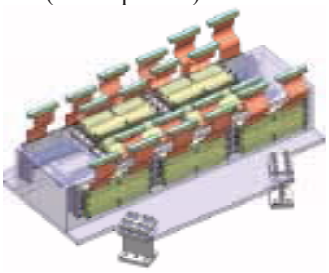

Fig. 1. Focal plane assembly

The PAN detection line is constituted of 5 TDI mode CCD arrays, whose pixels are PhotoMOS type with lateral anti-blooming structure.
The colored/multispectral bands (XS) are constituted of 5 CCD four linear arrays. The spacing between the centers of each line and the next is 936 µm allowing the necessary area for the readout registers and associated bus structures for each line. The photo-sensing elements of the XS pixels are photodiodes.
The focal plane assembly includes these 10 detectors which are equipped with flexible electrical links, optical mirrors which allow an optical and spectral separation,

and a SiC mechanical structural part which supports the detectors and the optical mirrors.

The focal plane SiC mechanical structure insures the stiffness and the geometrical quality of the two detection lines (PAN and XS), and allows the thermal regulation of the 10 detectors. The next figures shows the detectors mounted on the focal plane mechanical structure.

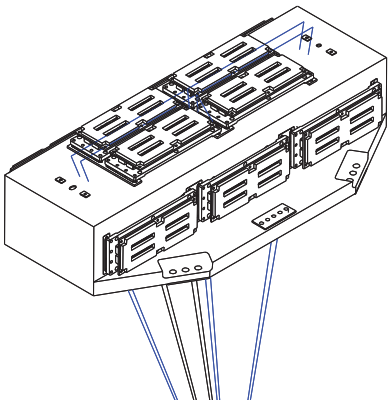

Fig. 2. Focal plane mechanical structure with detectors

Each detector has its own SiC mechanical frame which holds the detector ceramic package and the electrical connection which include some components mounted on a rigid circuit printed board and a flexible kapton link with a connector for interface with the detection electronics. This innovative architecture provides a versatile building block for a variety of imaging requirements.

The high integration level requires to use specific connecting parts : the link is made with flexible circuits optimized to operate at frequency close to 7 MHz and with the constraint of distance of typically 10 cm between the focal plane and the detection electronics.

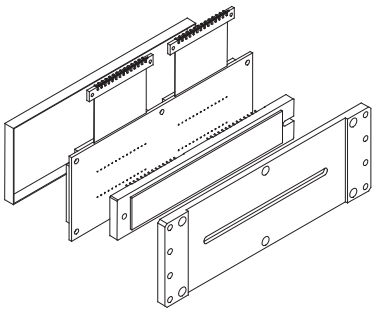

Fig. 3. Detector mechanical frame with electrical link

The two detection lines are 400 mm long. The specification of angular separation between PAN and XS (1.58 mrad maximum in the field separation) leaded to the implantation of a 400 mm splitting mirror in the focal plane. The focal plane also includes one butting mirror for each detector requiring two reflections in the optical diagram. This optical butting allow to have 2 perfectly aligned PAN and XS detector lines, with a very reduced separation between the two spectral bands.

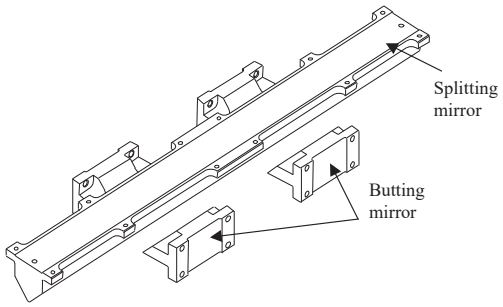

Fig. 4. Focal plane mirrors

One of the key features of the FPA is the extensive use of mechanical parts made of SiC. This material offers a very good thermal conductance leading to a simplified thermal concept, a low CTE for acceptable dimensional stability thanks to this class of camera featuring a low optics speed, and a very high mechanical rigidity for a low mass.

3. DETECTORS DESIGN

3.1 Panchromatic detector

The next figure shows the basic architecture of the panchromatic detector.

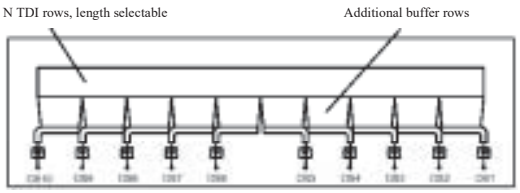

Fig. 5. Architecture of the panchromatic detector

The image section has 6000(H) x N(V) active pixels each 13 µm square and is clocked continuously to give a time-delay-and-integrate (TDI) function. The transfer of charge along the CCD is made synchronous with the velocity of the scan image. The integration time is N_i times longer than a single-detector integration time, where N_i is the number of TDI stages. Since the noise is proportional to $N_i^{1/2}$, the SNR improvement over a single detector is also $N_i^{1/2}$. Within the image section

are 4 separately connected electrode groups to enable the TDI length N_i to be varied.
Below the image section is a register that is split into 10 sections, each with a separate output circuit. The 5 sections on the right hand side transfer to the right and the 5 sections on the left hand side transfer to the left. Between the image section and the register are additional buffer rows with some of the buffer path slanted to make room for the output circuits. The last parallel transfer electrode is a transfer gate. At the top of the image section is a connection for the "antiblooming" drains that are necessary for the method of TDI length selection. The chip is left-right symmetrical about the central line.

The electrodes of the image section are of the four-phase type (designated $I\Phi_1$ to $I\Phi_4$). The clock sequences foreseen to be used for device operation causes charges to be stored under a pair of adjacent electrodes.

The method for varying the number of TDI stages is as follows. Down each inter columns isolation structure is a drain of type normally used for anti-blooming purposes. Four groups of $I\Phi_3$ electrodes are separately connected and designated A, B, C and D. These electrodes are normally clocked with $I\Phi_3$ but any group can be held at a suitably low constant voltage to block charge transfer down the array. Signal charge accumulates under the electrodes of the preceding pixel and any charge in excess of the full well capacity is lost in the drain. The TDI length is then the number of pixel rows in the normally clocked image section below the selected group. Any selected group can always revert to normal clocking and others be selected to change TDI length, but time may have to elapse for the charge accumulated in electrodes of the pixel above the first selected group to be blocked out before correct operation re-established.

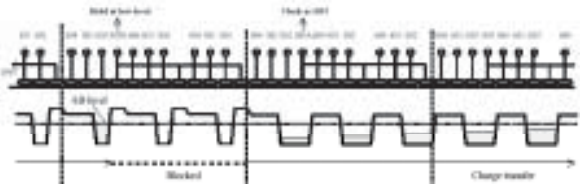

Fig. 6. TDI length selection

The full-well capacity is set by the processing used to fabricate the device, specifically the channel doping and the anti-blooming "barrier height", i.e. the well depth at which charge spills to drain. Some adjustment of the capacity can be possible by adjustment of the drain voltage. The target value is a minimum of 130 k electrons.
Each electrode in the image section has capacitance to substrate and also, as a result of the method of vertical connections, to most of the other phases. The total load per phase is that to substrate plus the various inter-phase components. The values for the clocks $I\Phi_i$ are approximately 3 to 4 nF. These values have a very strong impact on the detector performances and on the detection electronics design as the effect of the resistance of the metal and polysilicon connecting tracks is to slow the rise and fall times of the drive pulses applied by the detection electronics. The worst case slowing is at the device center in the last row before the transfer gate. The RC time constant is however relatively short, estimated at 0,15 µs, with the result that very fast drive pulse edges the times for the internal waveforms to change between 10% and 90% levels will be no more than 0,5 µs.
The output circuit has a charge conversion factor of 2 µV/electron capable of sufficiently fast settling with 10 pF external load to give an output waveform with essentially flat reset and signal sampling intervals each of 20 ns (the video rate for the Pléiades is 6,5 Mpixels per second for each panchromatic detector ouput).

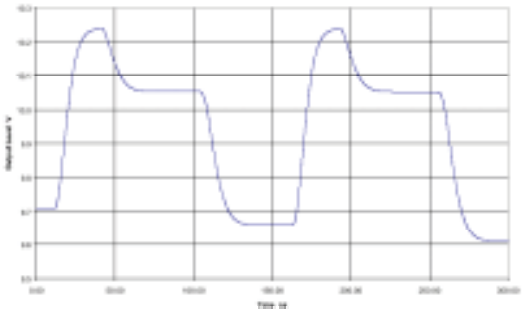

Fig. 7. Simulated output waveform

The dissipation value expected for each PAN device is 1,5 W total, with about 1 W on-chip.

3.2 Multispectral detector

For the multispectral detector, the photo-sensing element of the pixel is a photodiode. The detector consists of 4 lines of photodiodes, the spacing between the centers of each line and the next being 936 µm. Each line of pixels has 1,500 photo-elements on a 52 µm pitch and the size of each photo-element is 52 µm square. Signal charge generated in the photodiode is initially collected under an adjacent CCD electrode. Transfer of charge from the storage gate to the read-out register is performed by a transfer gate. An anti-blooming structure is implemented in the storage gate.
The register is a 2 phases structure, with a pitch of 26 µm. Each photo-element charges are stored under two pairs of adjacent electrodes ΦL_1-ΦL_2. Thus the readout register is operated at twice the required pixel frequency

(frequency of the ΦL_1-ΦL_2 clocks is 7,4 MHz) and the output signal is recovered after summing in the detector output stage.

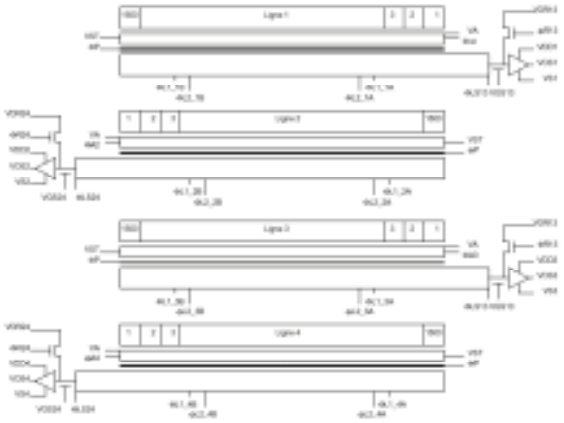

Fig. 8. Multispectral detector architecture

The antiblooming function can be adjusted separately for each pixel line. Each line is driven by 2 sets of specific electrodes ΦL_1-ΦL_2, which allow to deselect any of the 4 lines and reduce the power consumption of the chip.
Each pixel line has its own output, which lead to 4 output for the complete chip. The video rate is 3,7 Mpixels per second for each multispectral detector output.

The full-well capacity is far larger than the 130 k electrons minimum saturation requirement.

The values for the clocks ΦL_i are approximately 500 pF. This value is smaller that for the panchromatic detector as up to 8 pairs of ΦL_1-ΦL_2 can be driven on the XS detector.

The dissipation values expected for each XS device is about 2,5 W total, with about 1,2 W on-chip.

The standard detector package consists of a co-fired Aluminum Nitride (AlN) ceramic body with dual in line pins on the underside. The window is in BaK50 with an antireflection coating on both sides.

The spectral selection is made by optical filters placed very close in front of the detectors. XS strip lines filters (Fig. 9) are space-qualified multi-layer coating deposited on glass substrates. Each filter is composed of high-pass filter and low-pass filter. An absorbing material deposited between the XS filters isolates each band from the others to avoid inter-band stray-light.

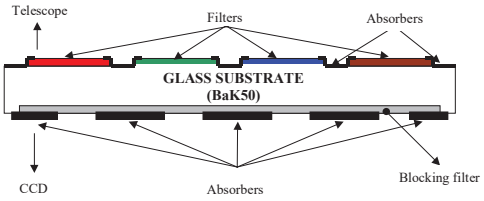

Fig. 9. XS filter design

4. ELECTRONICS DESIGN

The SEDHI concept requires to implement on a single board all electronic functions associated to 1 or 2 detectors, from the video signal pre-amplification to the digitization of video frame, and including various functions such as video signal processing, detector low noise power supply and polarization generation, detector and video processing chain sequencer, detector clock drivers, synchronization interface, command and control interfaces, …
The functional organization of this board, named MVP (Module Video de Proximité), is shown on the next figure. A full detection electronic is constituted of several MVPs, depending on number of detector in the focal plane, and a MSP board (Module de Servitude de Proximité), in charge of MVP synchronization and MVPs' interfaces with power supply and command and control equipment. Stacked MVPs and MSP constitute the detection electronic box. This box is mounted very close to the focal plane. Detectors are connected to detection electronics by the mean of short flexible printed circuits.
One MVP is able to process up to 10 CCD outputs, at a maximum pixel rate of 10 megapixel per second. Furthermore, due to high pixel frequency, detector and video processing chain clocks must be phased with an accuracy of a few nanoseconds. For this purpose, MVPs include several programmable phase trimmers in CCD phase driver blocks and in video processing chains.

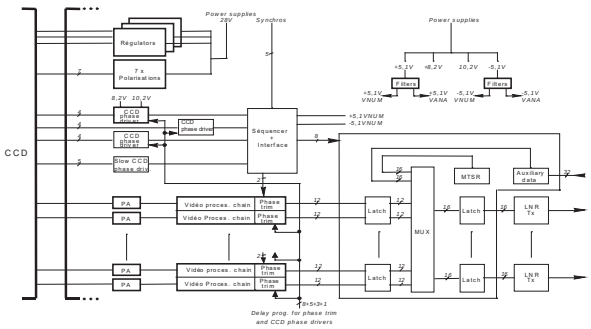

Fig. 10. Organization of a MVP

The high output data rate of a MVP (up to 1.2 Gigabit/ sec) is transmitted downstream through 2 LNTHD

(Liaison Numérique Très Haut Débit), which are serial integrated digital interfaces.
It must be noticed that there is a high level of modularity and standardization at the MVP level because one MVP is associated to one type of detector. With SEDHI architecture, the same MVP can be used each time the corresponding type of detector is used.

4.1 Technological implementation

Future high resolution instruments will require rather large quantities of few basic functions such as video processing chains, CCD phase drivers or LNTHD. For example, quantities are respectively estimated to 70, 220 and 30, in the case of one Pléiades camera.
Consequently, feasibility of these future instruments will depend strongly on the availability of those basic functions with good power and size budgets.
Unfortunately, standard component from manufacturers have scarcely the right characteristics, in term of functionality, performances or capability to withstand space environment. For video processing, CCD phase driving and digitally programmable delay no satisfactory standard component has been found. For this reason, CNES and Alcatel Space have chosen to develop 3 analogue/mixed ASICs corresponding to these 3 functions.
On the basis of these ASICs, two types of hybrids have also been developed : a video processing hybrid, and a CCD phase driver hybrid. These technological basic functions, ASIC or hybrids, are compatible with most detection electronic architectures, as described above. In that prospect, they can be considered as standard basic functions. Due to their low power and size budgets, these basic functions fulfil the requirements of limiting the mass, volume and power consumption of the complete subsystem which is one of the main goals of the SEDHI concept.
Technological implementation of next generation detection electronics is summarized on the next figure.

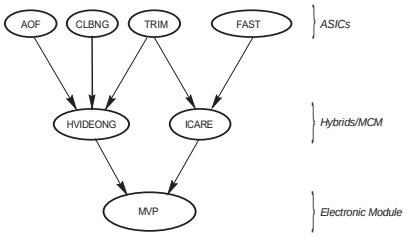

Fig. 11. Technological implementation

4.1.1 TRIM ASIC

The TRIM (Tetra Retardateur d'IMpulsion) is a digitally programmable delay, delay on rising edge and falling edge independent, 4 channels, in complementary BiCMOS technology.
The TRIM die includes 96 bipolar transistors, 4696 linear MOS transistors, 6772 logic MOS transistors, 85 diodes, 489 resistors and 408 capacitors. The die surface is 30 mm^2, and has 61 pads.
The TRIM main performances, measured at 25°C, are summarized in reference 2.

4.1.2 Video Processing ASIC (CLBNG)

The CLBNG (Cœur Large Bande Nouvelle Génération) performs a simple or double correlated sampling, 1 to 10 megapixel/s capability, two inputs, fully differential, internal reference, in complementary BiCMOS technology.
The CLBNG die includes 3565 bipolar transistors, 1570 linear MOS transistors, 349 diodes, 2313 resistors and 208 capacitors. The die surface is 47 mm^2, and has 94 pads.
The CLBNG main performances, measured at 25°C, are summarized in reference 2.

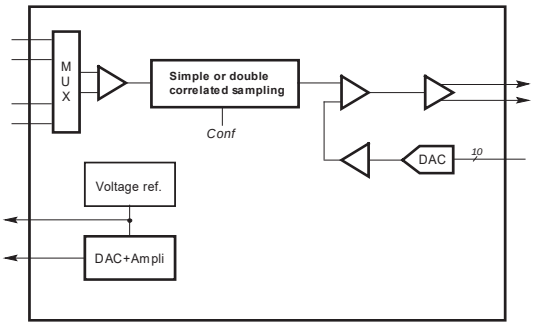

Fig. 12. CLBNG functional diagram

4.1.3 FAST ASIC

The FAST (Formattage et Amplification de Signaux Transitoires) is a two channels CCD phase driver able to handle capacitances up to 1.5 nF and 5 ns rising or falling edges, with digitally programmable rise and fall time (from 5 to 2 µs) and low and high output level, in complementary BiCMOS technology.
The FAST die includes 3609 bipolar transistors, 946 linear MOS transistors, 4376 logic MOS transistors, 82 diodes, 1500 resistors and 119 capacitors. The die surface is 45 mm^2, and has 63 pads.
The FAST main performances, measured at 25°C, are summarized in reference 2.

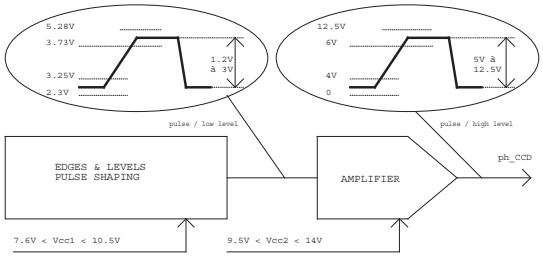

Fig. 13. Phase driving principle

4.1.4 HVIDEONG Hybrid

The HVIDEONG hybrid includes two complete video processing chains. Each processing chain is based on one CLBNG ASIC, one TRIM ASIC, one 12 bit 10 MSPS A to D Converter (ADC) from the commercial market, one digital ASIC for offset correction processing (AOF) and few other active and passive components. Compared to video processing chain of SPOT generation, these new chains exhibit a gain of two for the maximum pixel frequency and a gain of five for power and even more for size.

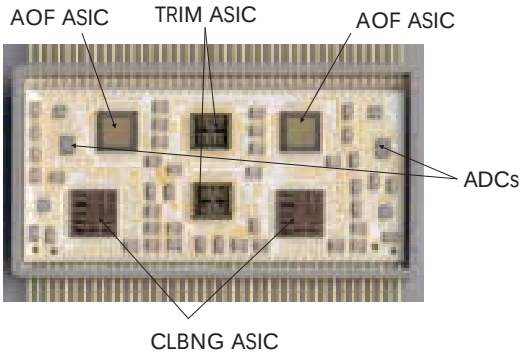

Fig. 14. HVIDEONG Hybrid

4.1.5 ICARE Hybrid

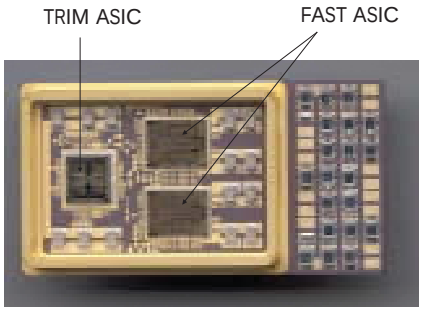

Fig. 15. ICARE Hybrid

The ICARE (Impulsions CAlibrées REtardées) hybrid is able to drive 4 CCD phases, and is based on 2 FASTs, one TRIM and few passive components.

4.2 Description of the video modules

Each MVP is constituted of 2 modules:

- the EGP (Electronique de Grande Proximité) module which includes the ICARE hybrids, preamplifiers for the detector outputs.
- The EMP (Electronique de Moyenne Proximité) module which integrates all the remaining detection functions, and the CCD power supplies distribution.

These two modules are embedded in a mechanical frame, and connected with a rigid printed circuit board. The connection between the CCD and the MVP is performed with a flexible printed circuit which will be the electrical interface between the focal plane and the detection electronics.
The possibility of adjusting the cable length authorizes to have a large number of CCDs in order to constitute very large focal planes.
The main performances tested on the MVP modules have been described in reference 2.

5. SEDHI FOR PLEIADES

5.1 Mechanical concept

The mechanical and thermal architecture is split in three distinguish parts corresponding to separate hardware modules: the focal plane, the electronics modules, the focal plane radiator.
Each element is supported independently by the telescope's structure with the help of mechanical frames and supporting blades.
Several configurations of focal plane may be considered depending on the application, and for Pléiades one will consider optically butted linear detectors.
The focal plane structure holds the detectors and insures the thermal conductivity between the detectors and the external thermal drain. The thermal flux dissipated by the detectors are dissipated in space through the focal plane space radiator.
Each electronics PCB is mounted in an individual mechanical frame to constitute a MVP. These modules are stacked together and screwed on a specific mechanical frame. The following figure shows the MVP mechanical package.

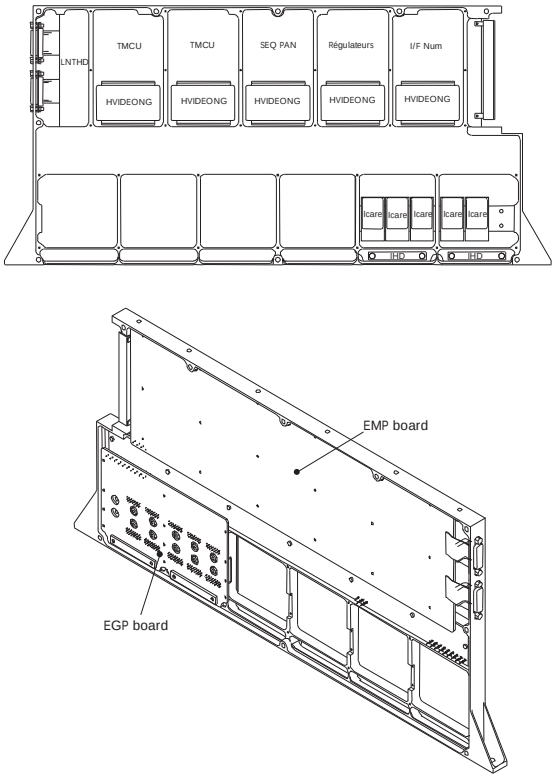

Fig. 16. MVP mechanical package

This architecture authorizes a very flexible mechanical architecture, which can be easily adapted to a wide range of focal plane requirements (number of detectors, length of the focal plane..), with a minimization of engineering efforts.

5.2 Thermal concept

The thermal concept must handle the heat generated by the detectors in the focal plane and by the MVPs.
The focal plane radiator size depends directly on the detectors power dissipation which is directly related to their operating frequency. The radiator sketched on figure showing the complete SEDHI must handle a detector power dissipation close to 20 W. The focal plane structure is thermally coupled to the radiator by cooper wires and/or heat pipes. The radiator is fixed on the telescope structure by insulation blades.
The MVP are thermally regulated by the radiated surface opposite to the MVP mechanical interface. The available surface is sufficient to limit the temperature of each module to a temperature compatible with the radiometric requirements. No thermal drain is required as the heat is conducted through the mechanical structure of each MVP.

5.3 SEDHI for Pléiades

The concept of SEDHI can be advantageously used for instrument with a high number of detectors like Pléiades.
The full detection electronics consist in 5 panchromatic MVPs, 3 multispectral MVPs, 3 panchromatic MSP (embedded in a single mechanical module) and 1 multispectral MSP. The Pléiades instrument electronics include the MVP functions, the MSP (Module de Servitude de Proximité) and the MSI (Module de Servitude Instrument) dedicated to command / control.
The PAN detection electronics is divided in 3 blocks:

- 1 block which includes 2 MVPs and 1 MSP
- 1 block which includes 1 MVP (associated to the panchromatic detector in the center of the focal plane) and 1 MSP
- 1 block which includes 2 MVPs and 1 MSP

The XS detection electronics is constituted of 3 MVPs (one of them associated to a single XS detector) and 1 MSP.

Each MVP PAN may provide up to 20 clocks to the PAN detector (24 for the MVP XS). Each clock is transmitted on a line which is specifically adapted, taking into account the connector and CCD input impedances.
The video interfaces between the detector outputs and the MVP are pseudo-differential, which is the best choice for Pléiades due to the electrical and thermal constraints.

All the sequencing functions of the MVP are integrated in a digital ASIC called SAPHO, which is common to PAN and XS and which can be easily configured for each of the sequencing modes. This ASIC receives the master clock from the MSP, and generates all the clocks required for the detectors, video processing and digital outputs synchronization. It also receives from the MSP the configuration data for mode selection and initialization of all parameters.

The video data after digitization by the Analog to Digital Converters in the HVIDEONG hybrids are transmitted to the Pléiades Compression Unit in the satellite. The data formatting and the transmission via High Speed Data link (LNTHD) is performed with a digital ASIC called MURANO. This ASIC also generates test pattern and it performs the multiplexing of the 12 bits of each of the video channels (5 for PAN,

each MVP PAN having 2 LNTHD, and 4 for XS, each MVP XS having 2 LNTHD). Each LNTHD is redounded.

Due to the very high level of integration, a large number of critical signals are transmitted inside each MVP: high speed clocks, high speed digital links, phase trimming clocks, video signals, high level CCD clocks. In order to guarantee the integrity of each of these signals, and to limit the possible effects of close neighboring of critical signals, many precautions have been taken. They include an important segregation of functions of different type, the use of adapted links (differential or pseudo-differential), the optimization of parasitic capacitance and the use of signal integrity and simulation tools to analyze and optimize the electrical diagram.

The main budgets associated to the Pléiades detection electronics are summarized on next table.

Parameter	Performance
Number of PAN video chains	50 at 6.5 Mpixel/s each
Number of multispectral video chains	20 at 3.7 Mpixel/s each
Output data rate	6.2 Gbits/s (useful rate 4,3 Gbits/s)
Mass	17 kg typical
Dimensions	463 mm x 237 mm x 246 mm
Power consumption	218 W

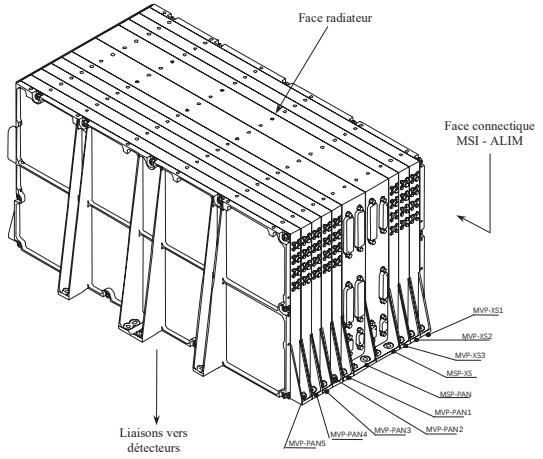

Fig. 17. View of the complete detection electronics

6. CONCLUSIONS

Alcatel Space has developed with CNES a new concept of highly integrated detection electronics, SEDHI.
The main advantages of this concept are the compatibility with the requirements of new generation of earth observation optical systems (large swath width, reduced ground sampling distance, number of spectral bands,…), the modularity, the compatibility with a large scale of missions, and the optimization of the engineering and manufacturing efforts during the development of an optical payload.
This "photon in – bit out" concept may be summarized by: radiometric performance optimization at lowest costs.
SEDHI has been selected by CNES for the Pléiades mission.

Fig. 18. View of the Pléiades SEDHI (including the focal plane and the radiators)

8. ACKNOLEDGMENTS

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8. REFERENCES

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