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Preliminary performances measured on a CMOS long linear array for space application

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PRELIMINARY PERFORMANCES MEASURED ON A CMOS LONG LINEAR ARRAY FOR SPACE APPLICATION

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ABSTRACT

This paper presents the design and the preliminary performances of a CMOS linear array, resulting from collaboration between Alcatel Alenia Space and Cypress Semiconductor BVBA, which takes advantage of emerging potentialities of CMOS technologies [1].

This CMOS sensor allows to address applications requiring:
- TDI capability coupled to image acquisition in pushbroom mode in order to enhance radiometric performances,
- Very long linear arrays thanks to stitching techniques,
- A high level of on-chip integration with both panchromatic TDI and multispectral linear sensors,
- On-chip correlated double sampling for low noise operation.

The design of the sensor is presented: it includes 8000 panchromatic pixels with up to 25 rows used in TDI mode, and 4 lines of 2000 pixels for multispectral imaging. Main system requirements and detector trade-offs are recalled, and the preliminary test results obtained with a first generation prototype are summarized and compared with predicted performances.

1   INTRODUCTION

The long linear CMOS detector is a Panchromatic (PAN)-Multispectral (XS) detector including 2 sets of pixel lines:
- The PAN pixel line which includes a Time Delay Integration (TDI) function with up to 25 stages
- The XS pixel line which is constituted of 4 parallel lines of pixels, each one corresponding to a specific colour.

This sensor is foreseen to be integrated in the future High Resolution (HR) Earth Observation Instrument focal planes.
Image acquisition in pushbroom mode coupled to TDI capabilities allows the enhancement of HR imaging radiometric performance, and the implementation of the PAN and the XS pixels on the same die allows an higher level of integration than other detector technologies.

2   MAIN REQUIREMENTS

The silicon ship requirements for the CMOS long linear array must include the following functions:
- the PAN imaging area, made of photosensitive cells, arranged in lines and columns into a Time Delay Integration (TDI) array,

PAN image area characteristics

Pitch along X (across scan)	13 µm
Pitch along Y (along scan, or along TDI direction)	13 µm
Number of photoelements per line	8000
Number of active line (operated in TDI)	8- 25

- the PAN readout circuit for Correlated Double Sampling (CDS), addition, multiplexing, single ended outputs, and associated logic and analogue functions,
- the XS imaging area, made up of photosensitive cells positioned close to the PAN image area, arranged in 4 linear arrays,

XS image area characteristics

Geometric dimension of a photoelement	52 µm x 52 µm
XS pitch along X (across scan)	52 µm
Number of photoelements per XS line	2000
Number of XS lines	4
Distance between adjacent XS lines (centre to centre)	20 x (XS pitch along x)
Distance between closest XS line and PAN line (centre to centre)	20 x (XS pitch along x)

- the XS readout circuits for CDS, multiplexing, differential outputs, and associated logic and analogue functions.

A ceramic package interfaces structurally, thermally and electrically the die with the system.

The long linear CMOS detector must be compatible with the following operating modes:
- PAN TDI and XS,
- PAN in staring mode (readout of one or several PAN lines without TDI summation) and XS. This mode is required for accurate MTF measurements which cannot be performed in TDI mode.
- Offset calibration mode (with reference signals inside the detector)
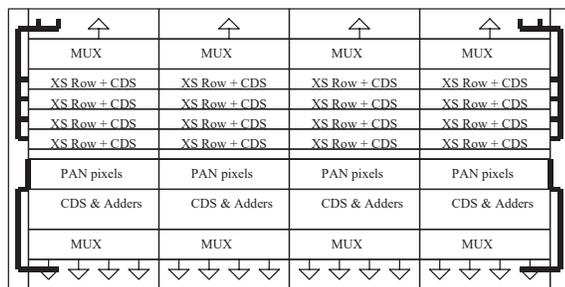
Fig 1 presents the sensor floor plan.

Fig. 1. PAN-XS CMOS floor plan

3   MAIN DESIGN TRADE-OFF

In order to optimize the global performance of the sensor (noise, response, MTF,…), several trade offs have been performed.
The main trade off concerned the pixel structure.
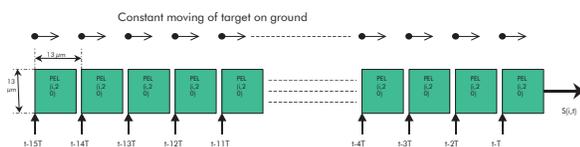The pixel topology finally used for PAN image area is shown [2].

Fig. 2. PAN sensor pixel topology

Pixel size has been optimized considering a maximum size of 13 µm and a minimum size of 10 µm which was preferred in a first approach, based only on optical constraints. A size of 13 µm has finally been selected, mainly because of the area required for the column circuitry. A larger pixel has also a better fill factor. These choices have been consolidated by elementary tests performed on test structures.

The integration of both PAN and XS lines has been demonstrated to be feasible without impacting significantly the yield.

PAN signal conditioning was also the result of a trade off. It contains a real CDS in order to optimize linearity and noise performances (reduction of the kTC noise). It means that for each PAN photo-element, a CDS circuit takes the reset level and signal level and yields the difference between both.
Signal conditioning contains dedicated signal operators, such as:
- preamplification with 2 possible gains to optimize performances in the complete range of line time
- offset correction electrical reference / stimuli
- sample & hold and associated switches
- analog multiplexing

4   SENSOR ARCHITECTURE

4.1   Panchromatic sensor architecture

The PAN sensor shall be able to perform a TDI function with up to 25 physical pixels. The sensor has four modes of operation:
- Offset calibration mode. An electrical black reference is used instead of pixels outputs during a normal grabbing sequence, the system could then sense every stage offsets.
- Staring mode. No addition is performed (addition of one sample only).
- Acquisition without transparent calibration.
- Acquisition with transparent calibration.

The pixel array size is 8000x25 (pitch: 13µm). Together with the associated 8000 columns performing CDS and TDI functions, pixels are controlled by a buffered decoder. The 8000 columns outputs are multiplexed by group of 500 on 16 outputs. This operation is controlled by horizontal shift registers.
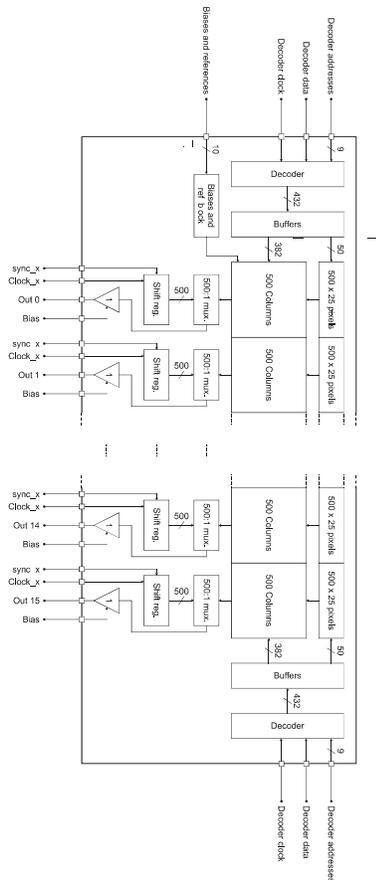
Fig. 3. PAN sensor architecture

A column contains:
- 25 pixels,
- a preamplifier, with two gains (1 and 2.75),
- 27 TDI stages, made of a CDS stage, an adder stage and a calibration stage,
- a multiplexer.

After proper sampling of the light information onto the photodiode capacitor, the signal is handled by the read out chain. Pixel reset and signal levels are multiplexed to the column bus, and sampled by a CDS stage.
This stage performs a subtraction of the reset level to the signal level, and feed the ktC noise free sample to the adder. When additions are completed, signals of 500 columns are multiplexed to an output buffer.
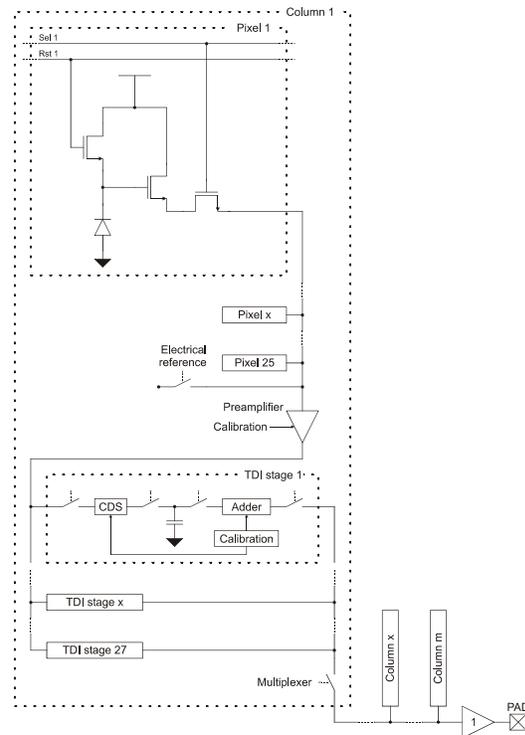
Fig. 4. PAN sensor column architecture

4.2 Multispectral sensor architecture

The XS sensor has four identical lines having a pitch a 1.04 mm (same pitch between line 1 and PAN pixel 1). Horizontal pitch is 52µm. The four lines are operated together, having their integration time starting and stopping synchronously (snapshot). Each line is then read one by one during the next integration period.

Fig 5 gives the architecture of the sensor.
Each pixel has a local amplifier and pseudo differential sample and hold stages. The four pixels of a column are then multiplexed to two outputs, one for the signal level and one for the reset level. Correlated reset and signal levels are multiplexed per group of 500, separately for reset en signal level. The subtraction by the system of the two outputs should give a ktC noise free signal.
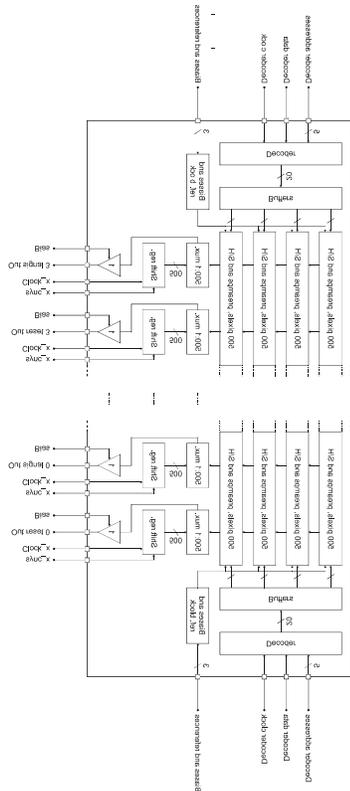
Fig. 5. XS sensor architecture

Fig. 6. XS sensor column architecture

A column contains:
- 4 pixels,
- a preamplifier, with three gains and 3 S/H stages per pixels,
- a multiplexer.

Because specifications between PAN and XS sensors are fundamentally different, column circuits are quite different as well. The reset and signal levels subtraction is done by the preamplifier. In order to reduce other source of noise (coupling…), the sensor provides pseudo-differential outputs. This sensor is essentially made of four linear arrays divided in four [500*4] arrays, due to the extra spacing required between lines. This allows an alternative approach for the pixel design.
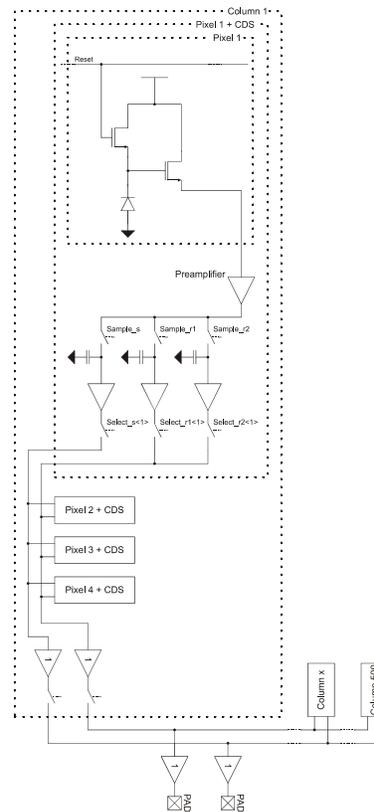
4.3   Sensor Technology

Target technology is the XFAB 0.35µm standard CMOS flow. The die area, which is larger than the maximal reticule area, requires that the sensor is fabricated using "stitching" technology. The device is divided into several basic blocks which are repeated and aligned together during photocomposition.

Both sensors are packaged in a single ceramic pin grid array (PGA) made of alumina (Al_2O_3).
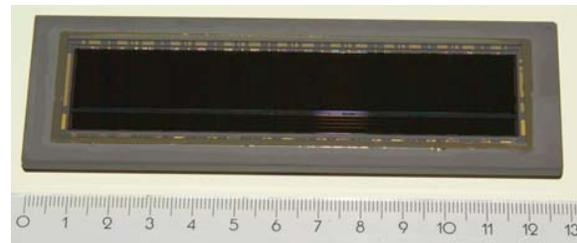

Fig. 7. View of the sensor in PGA package.

5   PRELIMINARY PERFORMANCES

5.1   Quantum efficiency

In order to optimize quantum efficiency, the wafer epitaxial layer is 7 μm thick with a peak QE at around 600 nm. The measurement results show QE x FF in the range [48%-53%] for spectral band [400nm-900nm]. These results are in line with a predicted high fill factor [2].

PAN-XS QE x FF average performances

	PAN pixel	XS pixel
[470-830] nm	0.52	0.58
[400-900] nm	0.48	0.53

5.2   Conversion factor.

PAN conversion factor results are independent versus NTDI as shown in Fig. 8. XS and PAN results are closed to predicted values.

PAN-XS conversion factor performances

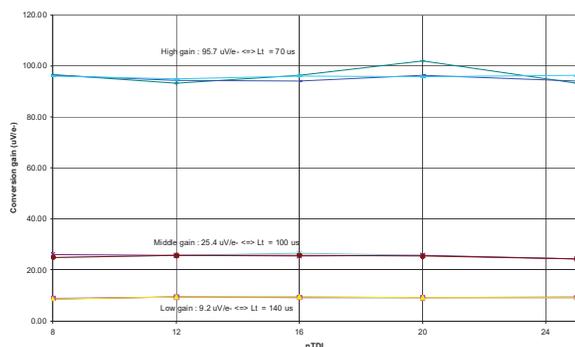| Gain setting	Conversion gain (μV/e⁻)		Corresponding L_T (μs)
	PAN	XS	
High	95	52	70
Intermediate	25	38	100
Low	9	14	140

Fig. 8. PAN conversion factor versus N_{TDI}

5.3   Photo response non uniformity.

Fig. 9. shows the average intra-stitch block PRNU versus nTDI for the three gain modes. It shows a maximum PRNU value of about 6.5%.
Remarkable is the increase with nTDI for the high gain mode. The effect is probably caused by a variation of some capacitive load with nTDI.
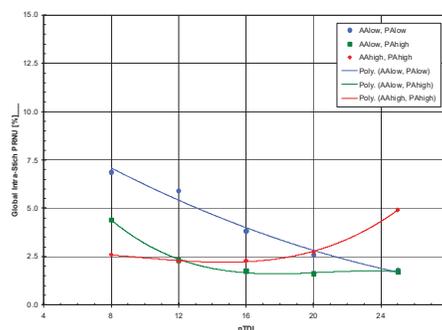

Fig. 9. Average intra-stitch block PAN PRNU versus nTDI for different gain modes

Fig. 10. shows the extracted PRNU values for the three gain modes of the XS and all PRNU definitions regarding stitching technology.
- inter-stitch block PRNU: PRNU variation over the different stitch blocks / outputs
- global intra-stitch block PRNU: averaged PRNU variation within each stitch block,
- local intra-stitch block PRNU : averaged PRNU variation within windows of 20x20
- intra-row PRNU: averaged PRNU variation within a row of a stitch block
- inter-row PRNU : averaged PRNU variation between the row.

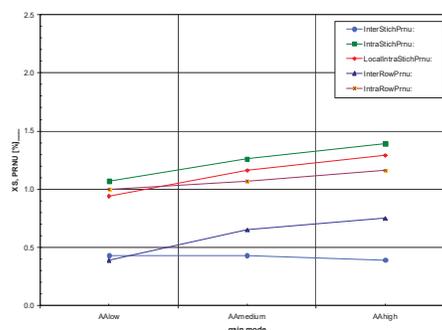A maximum value of less than 1.5% is obtained.

Fig. 10. XS PRNU values for the three gain modes.

5.4   Noise

The noise is measured in the voltage domain. Conversion gain figures are used to express the noise in electrons.

XS noise results are slightly different from noise predictions.

XS noise versus gain

	Noise (e-)	Noise (mV)
High gain	33	1,7
Middle gain	32	1,2
Low gain	41	0,6

PAN noise is higher than predicated, but still below the specification of 30 e- for 2 out of 3 gain modes, even for nTDI 25. Fig. 11. shows the results graphically. The slope of the noise curves is clearly different than predicted
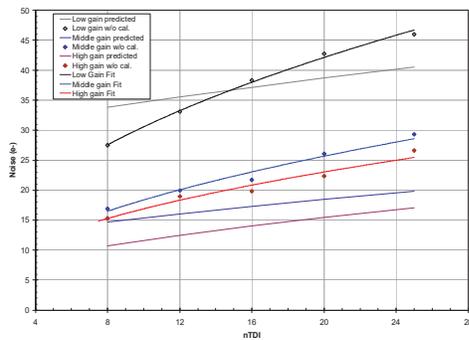

Fig. 11. PAN noise versus TDI number

5.5 Dark current and dark signal non uniformity.

Only the dark current values for the longest exposure and the highest temperature are significant. At 80 degC, 3.36 mV is measured, or 168 mV/s dark current with a standard deviation of 147 mV/s (DSNU). This indicates that the dark current is far below the specification of 1 nA/cm2 (~1 V/s) at 15 degC.

5.6 Dynamic range and non linearity.

The PAN linearity was measured for all NTDI and gain configurations.
In each case, linearity is better than 2% in the performance irradiance range [E1-E3] and better than 10% in the useful irradiance range [E1-E4].

The saturation level is a function of NTDI. For low value of NTDI, saturation is due to pixel saturation level. For high NTDI value, CDS and adder saturate before pixel level.
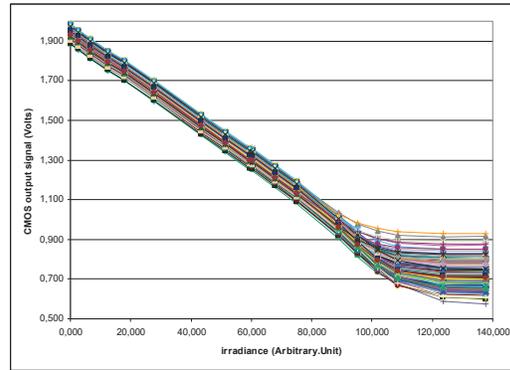

Fig. 12. Preliminary PAN pixel response curves with high preamp gain low adder gain (NTDI=8)

Similar to the response measurements on the PAN, measurements were carried out for the XS.

5.7 Fixed pattern noise (FPN).

For nTDI equals 8, 12, 16, 20 and 25, the FPN has been measured on a complete image without calibration mode. As expected, the dominant source of FPN is the TDI stage. But calibration mode keeps the nominal mode and optimization and characterization of this calibration function are in progress.
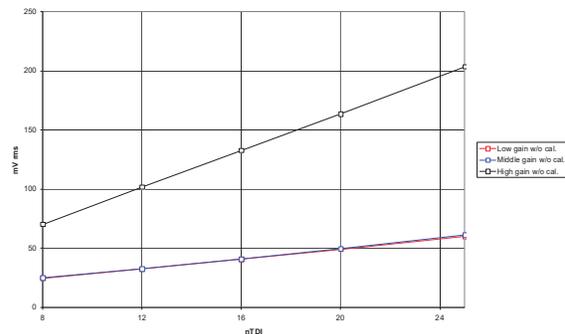

Fig. 13. Global PAN FPN without calibration

Preliminary promising results using calibration mode present a large decrease of PAN FPN. For NTDI=8, a 3mV rms global FPN level was measured with calibration mode compared to 70 mV rms without calibration mode.

XS FPN has been measured on a complete image, per row, per output and per both row and output. As expected, the dominant source of FPN for this case is the buffer associated with each pixel.

XS FPN

mV rms	Low gain	Middle gain	High gain
Global FPN	18	20	21
Line FPN	18	20	21

6   NEXT STEPS

After a design and manufacturing phase and electro-optic characterisation of a complete prototype lot of PAN-XS, complementary characterisations are currently performed using dedicated test bench which will allow to identify precisely the performance of such sensor, and to perform the feed-back on the sensor design with the objective of embedding such sensor in the next generation instruments developed by Alcatel Alenia Space

7   CONCLUSION

Design of a TDI sensor in CMOS technology has been demonstrated. This chip is based on two different architecture sensors to combine high resolution PAN TDI acquisition and multi spectral imaging for pushbroom mode. Preliminary radiometric performances are closed to requirements. Key performances like noise, linearity and non uniformity photo-response show very interesting results with respect to system requirements. Moreover some studies and complementary characterisations will be done to optimize and enhance the performance of such a new generation CMOS long linear array.

8   REFERENCES

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2. US patent No 6,225,670, B. Dierickx, G. Meynants, D. Scheffer, *Near 100% fill factor CMOS active pixels*, IEEE CCD & AIS workshop, Brugge, Belgium, 5-7 june (1997); Proceedings p. P1.