

# Why did Intel fail with 60 nanometers? Reiteration of the noise, information, speed and heat aspects of the breakdown of Moore's Law

Laszlo B. Kish and Yingfeng Li

Department of Electrical Engineering, Texas A&M University  
College Station, Texas 77843-3128, USA

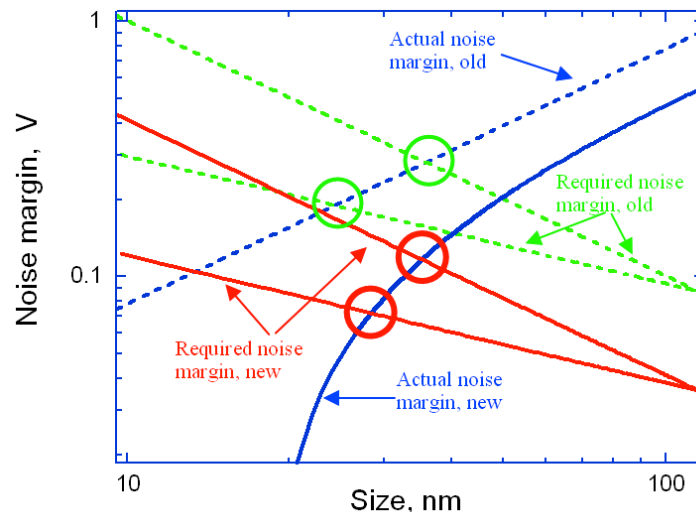
## ABSTRACT

The evolution of microprocessor miniaturization and performance, often described by Moore's law<sup>1,2</sup>, is close to the saturation limit. This is the part of a more general slowing down which is indicated by, among other things, the facts that Intel has failed with the 65 nm efforts and IBM has recently given up its personal computer market. In the present paper we would like to discuss some noise-related characteristic features of the present situation from the angle of noise and dissipation.

*Keywords:* leak current, Moore's law, power dissipation, switching noises, thermal noise

## EARLY BREAK OF MOORE'S LAW

Concerning fundamental physical principles, Statistical Physics is at hand to pose limits on Moore's law and on the performance of processors. In 2002, it was predicted<sup>3</sup> by one of us that the synergic effects of the increasing thermal noise, heat dissipation and bandwidth during miniaturization would manifest in either a high bit-error rate or chip overheating eventually. Ralph Cavin, the Vice Director of Semiconductor Research Corporation, has basically arrived at similar conclusions in his presentations while approaching the problem from other angles<sup>4</sup>. Based on recent trends, an estimation was made<sup>3</sup> and this noise-based break of Moore's law was predicted to take place around 30-40 nanometers, which was expected to be reached around 2008-2010. Figure 1 shows the original and the refined predications.



**Figure 1.** The original<sup>1</sup> and the refined predictions. The refined prediction takes into the account the more realistic (lower) supply voltage, the CMOS threshold voltage and efforts to reduce the supply voltage less rapidly. Even though the last effort is questionable because of the already too high electrical field, the predicted size range of the break turns out to be very similar in the old and the new prediction. The required noise margins have two asymptotic lines in both cases which are dictated by simple physical limits of changing gate oxide geometry<sup>1</sup>.

Surprisingly, a break of Moore's law took place much earlier, at the summer of 2004, when Intel failed with moving from 90 to 60 nanometers. In the media, reports were talking about *heat, bit-errors* and leakage current problems. The ultimate solution was that Intel abandoned the miniaturization for the moment and was considering buying an AMD's processor with 115 nanometer characteristic device length for the next generation of PCs, which was a *step-back with miniaturization or integration density*. As a consequence, the *clock frequency was reduced*. This situation was an apparent break of Moore's law already at 60 nanometers, and only the future can show if it is a temporary break or ultimate failure. It is tempting to cite here the beginning of the Conclusion section of paper<sup>3</sup> about the major impact of the statistical physical arguments. Comparison of the bold-printed terms in the text above and below is showing a striking relevance:

*"It is important to emphasize here the nature of the problem. The arguments in this paper do not set any physical limit on transistor sizes. What is claimed here, the logical threshold voltage, therefore the supply voltage, cannot be reduced below a certain limit due to false bit-flips induced by thermal noise. The only way to get around this effect would be either giving up to increase the integration density, that is itself Moore's law, or giving up to increase the clock frequency. However, that would be contradictory because increasing the clock frequency is one of the most important reasons for the miniaturization efforts. For the sake of simplicity and generality, we used several strong approximations during these considerations. Most of the approximations were optimistic, so the real situation is probably worse..."*<sup>3</sup>

### WHY SO EARLY ?

However, it is important to ask why Moore's law broke so early? Our interpretation of the situation is the following. A sufficient reason is the progressively decreasing bit/J energy efficiency due to the leakage current, which was not considered<sup>3</sup>. If the total power dissipation is dominated by leakage current, the energy efficiency is reduced exponentially due to the miniaturization.

The prediction<sup>3</sup> has inherently supposed that the energy efficiency of the bit operations (measured in bit/J) stays constant in the future, which is not true for leakage current dominated dissipation. Using level crossing statistics to estimate false bit events, which is more reasonable than earlier statistical methods based on error function or entropy calculations, as was shown in Equation A8 of paper<sup>5</sup>, that the processor dissipation scales with characteristic device size  $d$ , clock frequency  $f_c$  and bit error probability  $\epsilon_c$  as

$$P_{total,min} = -Nf_c kT \ln[(\sqrt{3}/2)\epsilon_c] = -Fd^{-2}f_c kT \ln[(\sqrt{3}/2)\epsilon_c] , \quad (1)$$

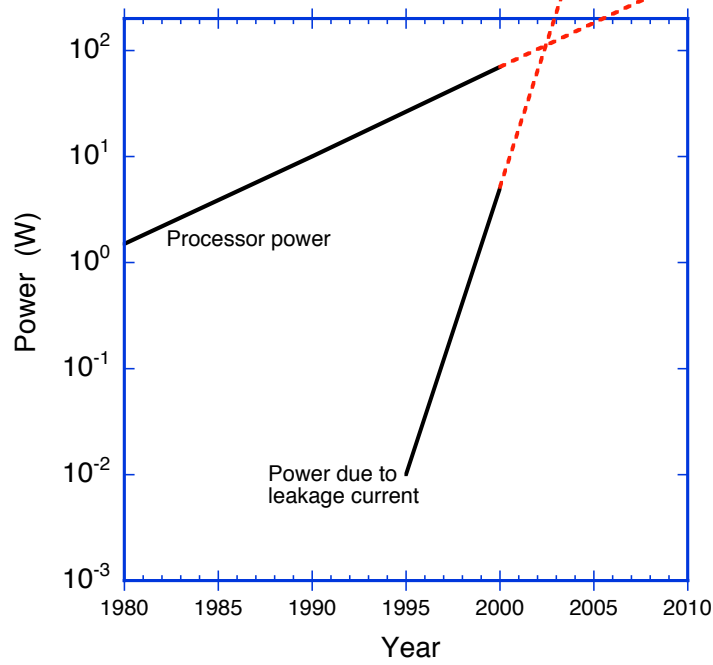
where  $F$  is a factor related to the bit/J energy efficiency of the processor<sup>5</sup>. This equation gives the minimal energy requirement of a classical processor, if any crossing of the noise margin causes a bit flip. By comparing this result to real processor heat, it is pointed out<sup>5</sup> that the energy efficiency is extremely low, presently about 0.1%.

In Figure 2, the extrapolation (dashed lines) of curve fits of processor power and leakage current power. The fit line is replotted (solid line) and extrapolated (dashed line) from Gordon Moore's presentation in 2003<sup>2</sup>. The crossing of the extrapolated lines indicates that the leakage current power becomes progressively dominant from around 2002-2003. The extrapolation indicates that, since about year 2000, the leakage current heat is dominating the power dissipation. Thus the prediction based on Fig 1 is too optimistic.

If we make a simplistic approach that the actual total dissipation is much larger than that and it is dominated by leakage current then we make the following estimation:

$$P_{total} = AU_s \exp\left(B \frac{U_s}{d}\right) \quad (2)$$

where  $A$  and  $B$  are constants,  $d$  is the characteristic size of the devices and  $U_s$  is the supply voltage. Equation (2) takes into the account the fact that the thermally activated tunneling current is an exponential function of the voltage and the inverse of the thickness of the oxide.



**Figure 2.** Extrapolation (dashed lines) of curve fits of processor power and leakage current power. Fit line re-plotted (solid line) and extrapolated (dashed line) from Gordon Moore's presentation in 2003<sup>2</sup>.

Then the energy efficiency can be given as:

$$\eta \cong \frac{-\frac{F}{d^2} f_c kT \ln\left(\frac{\sqrt{3}}{2} \epsilon_c\right)}{AU_s \exp\left(B \frac{U_s}{d}\right)}, \quad (3)$$

which can be summarized as

$$\eta = C \frac{f_c \ln\left(\frac{\sqrt{3}}{2} \epsilon_c\right)}{U_s \exp\left(B \frac{U_s}{d}\right)}. \quad (4)$$

Where  $C$  is a new constant. Of course, more can be said if we realize that there is a relation between the clock frequency  $f_c$  and the characteristic device size  $d$ .

If we assume that the gate oxide thickness is roughly scaling as  $t \propto \sqrt{d}$ , the gate capacitance scaling can be estimated as  $d^{3/2}$  which implies a scaling relation

$$f_c \propto d^{-3/2} \text{ or } d \propto f_c^{-2/3}, \quad (5)$$

which implies:

$$\eta = C \frac{f_c \ln\left(\frac{\sqrt{3}}{2} \epsilon_c\right)}{U_s \exp(BU_s f_c^{2/3})} \quad (6)$$

The denominator indicates progressively (exponentially) decreasing energy efficiency versus the clock frequency.

The energy efficiency is very low in today's microprocessors, so it seems, and there is plenty room to improve it. However, it seems that would require a completely different technology because the energy efficiency is radically decreasing. The dissipation of progressively growing leakage (tunneling) current during miniaturization has become dominant (see Figure 2) while approaching the 60 nanometer and radically decreased the bit efficiency. The leakage current is a quantum tunneling current, thus it grows exponentially with the shrinking oxide thickness. Because it is a thermally assisted tunneling process, it scales exponentially with the gate voltage, too. However, the thickness-exponent is much greater, thus the effect due to decreasing of the thickness is dominant, which manifest in a roughly exponentially evolving dissipation, see Figure 1. Because processor heat is close to its highest manageable level, to avoid overheating the processor, its supply voltage had to be decreased. This step implied a shrunk noise margin. It was shown<sup>3</sup> that a 10% reduction of the noise margin at today's bandwidth and transistor number increases the bit-error rate by a factor of  $3 \cdot 10^5$ . Most likely, a synergic combination of thermal noise and switching noises (cross-talk noise) cause the erroneous functioning.

### ACKNOWLEDGEMENTS

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