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RESEARCH PAPER

Detection of defective chips from nanostructures with a high-aspect ratio using hyperspectral imaging and deep learning

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ABSTRACT. We have developed an imaging spectroscopic reflectometry (ISR) method based on hyperspectral imaging and deep learning to detect defects in the bottom region of high-aspect-ratio nanostructures. ISR enables fast and non-destructive imaging of the bottom critical dimension (BCD) of channel holes (CHH) on a chip die of vertical NAND (V-NAND). A supervised learning model is built to predict the BCD by associating a pre-measured hyperspectral cube with scanning electron microscopy images after decapsulation of the top of the sample. The BCD predicted by ISR shows a high correlation of $R^2 = 0.72$ with the actual BCD, and the distribution of CHH not open (NOP) defects on the chip die identified by bright field inspection after decapsulation is consistent with the BCD image obtained by ISR. In addition, ISR can detect defects that occur at arbitrary positions relative to the optical critical dimension (OCD) of the die. On fully integrated V-NAND chips, the ISR result showed a high correlation ($R^2 = 0.82$) with the failure rate caused by CHH NOP, while the conventional spot OCD showed only $R^2 = 0.41$. Thus, ISR can be used to optimize the etch process for weak wafer edge regions and to detect defective etch equipment.

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1 Introduction

Scatterometry, which measures the size of three-dimensional nanometer structures from the spectrum of light reflected from the surface of a sample, is known as optical critical dimension (OCD) and is currently the most utilized structural observation technique in the metrology process of integrated semiconductor mass production.[1–4] Techniques such as scanning electron microscopy (SEM), tunneling electron microscopy, and atomic force microscopy, which have a much higher spatial resolution than OCD, are known to have limitations in observing nanostructures. These limitations include the inability to obtain information in three dimensions, the requirement of lengthy measurement times to scan large areas, and the potential for sample damage.[5] By contrast, OCD based on spectral reflectance (SR) or spectroscopic ellipsometry (SE) offers several advantages. It employs near-visible light to measure the average size of a population of nanometer structures, it is non-destructive, and if the light source is in the infrared region, it can obtain information down to the bottom of high-aspect-ratio (HAR) structures.[6] In addition, the method

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is advantageous in that no sample preparation is required for measurement, and the measurement time is relatively brief, which facilitates statistical analysis through repeated measurements. However, it should be noted that, traditionally, OCD is a spot measurement technique, meaning that it does not have spatial resolution over the two-dimensional plane of the object being measured. To obtain results for a given area, point-by-point measurements must be taken in succession and then combined.[7,8] The time required to measure all of the hundreds to thousands of chip dies formed on a 12-in. diameter Si wafer substrate is rather long, so only a few tens to dozens of points per wafer are sampled. However, this represents only 0.00001% of the bits generated on a single wafer. Consequently, if the process to be monitored exhibits a considerable degree of tolerance and the location of the defect is uncertain within the wafer or chip die, spot OCD will be unable to identify the defect.

Hyperspectral imaging is expected to overcome the shortcomings of spot OCD measurements.[9,10] Hyperspectral imaging acquires spectra with high spectral resolution over a wide range of wavelengths, collecting data from each pixel in the image. In other words, spectral information for OCD is collected from a large area simultaneously, so hyperspectral imaging can be used to evaluate the dimensions of nanostructures created on wafers over a large area simultaneously.[11] Samsung has developed a measurement and inspection technology called imaging spectroscopic reflectometry (ISR) based on supervised learning computation and hyperspectral imaging, which has been in development for about a decade.[12–18] Our ISR uses a spectral scanning method with a high-speed monochromator and is capable of measuring the entire wafer in about 2 h for dynamic random access memory (DRAM) process wafers. After the measurement, we use a pre-trained deep learning model to quickly obtain the structure size from the spectrum. This ability to quickly view the entire wafer makes ISR useful for optimizing the integration process of new products, where it can quickly identify suspect processes for defects by identifying characteristic patterns in the wafer gradient. In addition, in-chip uniformity can be obtained by measuring the chip die at once, which is useful for detecting defective chips when weak spots occur in the chip in various ways.[14] In particular, it is necessary to inspect the actual cell area directly over a large area to know the post-process status of the wafer edge area where no observation points are formed.

To achieve high yields in excess of 80% for volume products, it is essential to reduce the number of defective chips at the outer edge of the wafer, especially as semiconductor chips become smaller and the proportion of chips at the wafer edge increases. The development of etching processes, which are key to forming HAR structures and other processes, is becoming increasingly important at the wafer edge.[19] Edge exclusion has been steadily reduced by improvements such as temperature control near the wafer center and bevel, and differential radio frequency bias in the center and periphery. To understand the extent to which these fine process adjustments are successful, dimensional measurements of HAR structures over a large wafer area are required.

One product where HAR structures are becoming increasingly important is vertical NAND (V-NAND).[20] V-NAND, also known as 3D NAND, is a charge trap-based flash memory device that requires a vertical channel structure to be formed by drilling a mold with hundreds of layers of silicon oxide and silicon nitride (ON).[21–23] These holes are called channel holes (CHH), and with each generation of V-NAND, the number of layers increases, resulting in a very high HAR structure.[24] The etching process for drilling CHHs is therefore challenging, and it is even more difficult to form a normal shape of CHHs in the edge region of the wafer because the etching process conditions are different from those in the inner region.[25] In particular, not-open (NOP) defects, where the hole does not penetrate to the bottom layer, often occur at the edge of the wafer. Due to the high number of NOPs in the edge area, the thick ON mold can be torn off from a large area of the wafer in the subsequent process, resulting in the loss of many chips. Therefore, the wafer edge area is often excluded from CHH etching to avoid large losses.[26]

In this paper, we have used ISR technology to monitor etch defects on dies in the outer regions of the wafer for a generation of V-NAND products nearing process optimization. We show that ISR is capable of non-destructively measuring the bottom critical dimension (BCD) of CHH over a large area and that its ability to detect chips with CHH NOPs is superior to conventional spot OCD due to its large coverage capability. Therefore, we conclude that ISR can be used as a guide to optimize the etch process to reduce edge exclusion areas.

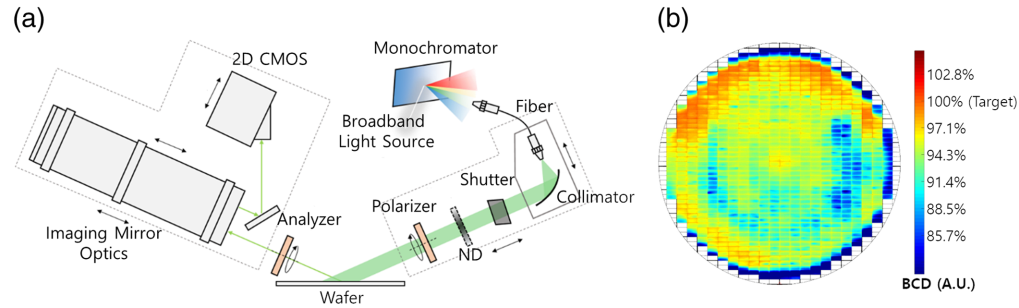

Fig. 1 (a) Optical configuration of ISR. (b) Example of CHH BCD image of a whole 12" radius wafer.

2 Methods

2.1 Optical Configuration of ISR

The optical components of the ISR used in this study are shown in Fig. 1(a). A laser-amplified plasma broadband white light source is used to obtain images at multiple wavelengths. The white light source is separated into each wavelength by a monochromator. The diffraction grating of the monochromator is synchronized with the camera while rotating at high speed to measure the monochromatic images. The spectroscopically decomposed light source is collimated as a plane wave and incident on the wafer, and the reflected light is collected by 0.08 numerical aperture (NA) and 1 magnification of the imaging optics. Then, a signal is recorded on the 2D complementary metal oxide semiconductor (CMOS) camera (Photometrics Prime BSI). Due to the quantum efficiency of the Si-based CMOS, the available wavelength range of ISR is 350 to 1100 nm. In this paper, the wavelength region used for V-NAND CHH evaluation was 550 to 1100 nm, and the image was measured at intervals of 2 nm. The field of view (FOV), which is the area measured at one time, can be up to the total area of CMOS ($9 \times 9\ \text{mm}^2$). This is 90,000 times larger than $30 \times 30\ \mu\text{m}^2$, which is the usual spot size of conventional. The spatial resolution can be as high as 6.5 μm, a CMOS pixel size, but has been reduced to 162.5μm by post-binning in consideration of data computation time. The reflectance spectrum, which is a raw signal of the ISR, is calculated by Eq. (1) by measuring the five points of the bare Si wafer before measuring each wafer, taking a median spectrum and using it as a reference signal. The actual FOV used in this study is $8 \times 5\ \text{mm}^2$, and as shown in Fig. 2(d), two of the four mats that make up the die of our V-NAND product can be measured simultaneously

$$\text{Reflectance}(x, y, \lambda) = \frac{\text{Sample}(x, y, \lambda)}{\text{Reference}(\lambda)}. \tag{1}$$

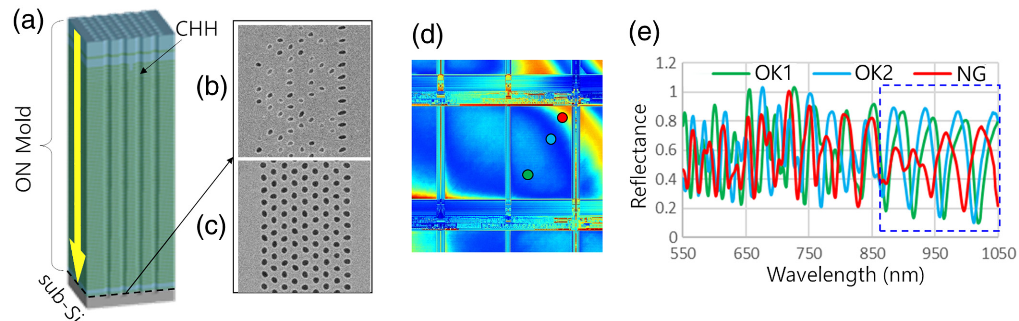

Fig. 2 (a) CHH structure of V-NAND. For the bottom CD inspection of CHH, the mold structure at the top is removed by decapsulation as much as the height indicated by the yellow arrow and the remaining hole is imaged by either an optical microscope or SEM. (b), (c) Decapsulation SEM images of the CHH of V-NAND at the chip outer region (b) and the central region (c) of the processing wafer. (d) Monochromic image ($\lambda = 550$ nm) taken by ISR of V-NAND chip. (e) ISR spectra at points of green, blue, and red are shown in Fig. 2(d), respectively.

2.2 Product Wafers for Evaluation and Supervised Learning Models for Signal Analysis

The evaluation was performed on a process wafer immediately after the etch process was performed on the ON-repeat stack to form the CHHs of the V-NAND. The BCD of the CHH is calculated and obtained by a deep learning model from the measured reflectance spectrum. After obtaining 12,000 ISR spectra from 30 device wafers of V-NAND, the SEM image was measured after decapsulation as shown in Figs. 2(a)–2(c) to obtain the diameter of the actual bottom CHH. A deep learning model was constructed by linking the ISR spectra with the hole size obtained from the SEM images. The deep learning model used a feed-forward neural network with two hidden layers, where the number of hidden nodes decreased by a rate of 0.8 from the previous layer. The epoch was set to 3000, with a learning rate of 0.001. The L2 regularization rate was set to 0.0001. A dropout of 20% was employed to prevent over-reliance on specific wavelength band information. In addition, data enhancement was performed by applying random noise of 0.2% of the spectral amplitude. It should be noted that for semiconductors, obtaining reference data is expensive due to the consumption of device wafers. Therefore, we are unable to use as much sample data as in typical deep learning cases. That is why our approach is to use basic nets rather than the latest complex models. To verify the model, as a post-test evaluation, additional device wafer samples not included in the learning parameter were measured by ISR and compared to the decapsulation SEM results.

The trend of CHH BCD was collected by measuring high-volume V-NAND production using ISR measurement as a metrology process step. After the integration processes of the chip on which the ISR was measured, the correlation between the sum of the defect rates related to the CHH NOP and the CHH BCD derived from the ISR was compared to confirm the reliability of the supervised model for the ISR.

3 Results and Discussion

3.1 Validation of Deep Learning Model for CHH BCD

After the CHH of V-NAND is formed by the etching process, the ISR spectra are shown in Fig. 2(e). Unlike the green or blue dots in Fig. 2(d), where the CHH BCD is good in the cell array region, the spectrum obtained from the red dots, where the CHH BCD is small and poor, shows a shape difference in the near-infrared region, 850 to 1100 nm. In the 550 to 850 nm region, however, the spectral shape difference is more difficult to identify, with no correlation between normal and abnormal locations. It can be concluded that the NIR region above 850 nm is dominant in detecting cases where the lower part of the CHH is blocked or somewhat narrow at the edge of the wafer. Therefore, it is expected that the visible spectrum with the available wavelength range of 370 to 750 nm will be insufficient to detect the corresponding CHH BCDs in the spectrum, indicating that the acquisition of spectral information in the near-infrared region is essential when targeting high HAR structures. Note that for the SE results in Secs. 3.3 and 3.4, we used a wider range of spectra than the wavelengths used by ISR, especially extending further towards the longer wavelengths.

To maintain the confidentiality of Samsung's product parameters, we will present the CHH BCD values in this paper as percentages of the design target critical dimension (CD), which is around $60 \sim 90$ Å, rather than the actual dimension. When the supervised learning model inferred the CHH BCD from the acquired ISR spectra, we obtained a correlation coefficient of determination, R^2, of 0.96 and a root mean square error (RMSE) of 0.95 Å, with a maximum error of 15.9%, for the test sample set in the BCD range of 60 to 107.1%, as shown in Fig. 3. We post-tested the model by measuring new additional samples for data not included in the training dataset and found a good agreement of $R^2 = 0.71$ with RMSE and maximum error of 2.72 Å and 25.2%, respectively, over the range 64.3% to 107.1%. The validation agreement was found to be worse for smaller BCDs, which is probably due to the fact that the region from which the spectra for smaller BCDs are obtained contains many cases where the bottom CHH is not formed, or the irregular shape of the hole leads to a decrease in the predictive power of the BCD as the spectral shape becomes irregular regardless of the CHH size.

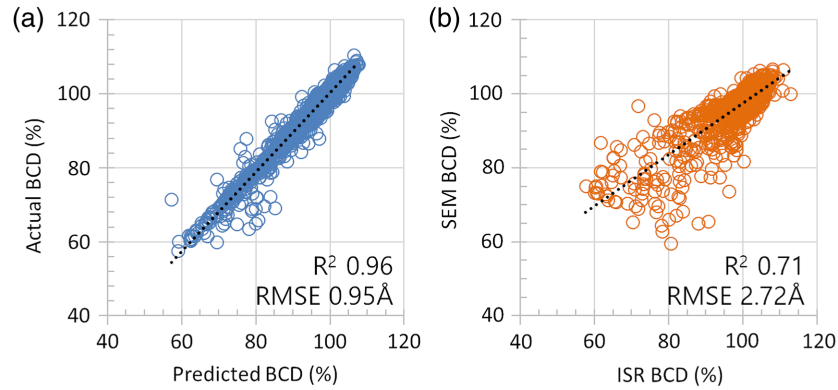

Fig. 3 Correlation between actual BCD and ISR results inferred by the supervised deep learning model. The test prediction (a) and verification prediction for additional samples (b).

It took about 4 months to accumulate 18,000 pairs of spectra and references as data sets for ISR-supervised learning and to optimize the model. Not only is this a long time to set up a metrology step for mass production, but it also requires the destruction of a large number of wafers to obtain references. In Samsung's own experience, when using SE spectra, where more information is preserved and various system noises are canceled out by the two different polarization signals, it typically takes about 1000 pairs of spectra and references from SEM images before a high correlation can be achieved by supervised learning with references obtained from SEM images. This means that the current ISR is relatively inefficient for building deep learning models. This is because ISR is based on SR signals, which have a relatively low information dimension and are susceptible to system noise. To overcome this shortcoming, it is necessary to upgrade the hardware of ISR to be based on SE signals,[18] to preprocess spectral signals, or to use artificial spectra as a reference for supervised learning.

3.2 Non-Destructive In-Chip BCD Imaging by ISR

The BCD gradient of CHH in chip die obtained from ISR is shown in Figs. 4(a) and 4(b). A sharp decrease in BCD is observed mainly in the corner regions away from the wafer center. For the same location on the same wafer, the gradient shape in the cell array region in Fig. 4(c), which shows the CHH NOP defect spots by optical microscopy inspection tool (KLA Discovery 7) after decapsulation, and Fig. 4(b), which shows the ISR results, are very consistent. As the ISR BCD decreases, the NOP defects detected by optical microscopy in the actual CHH bottom region

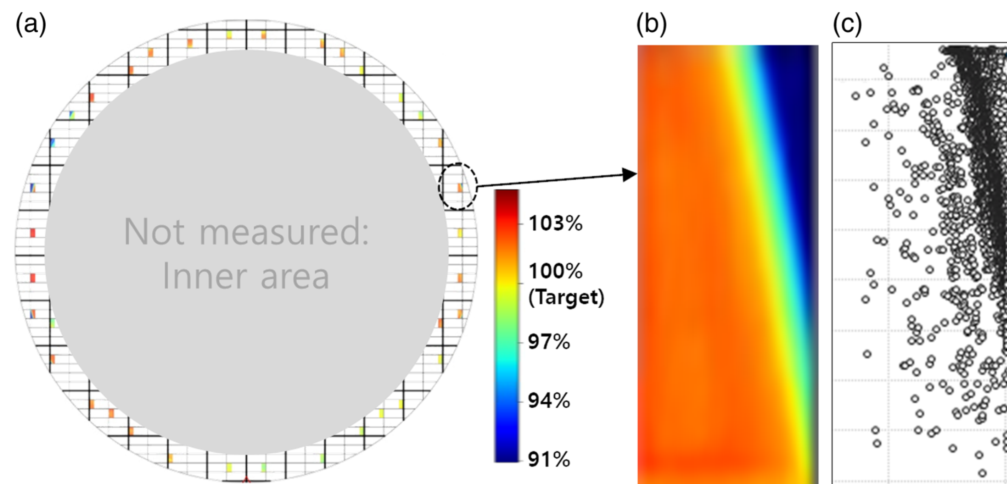

Fig. 4 (a) CHH BCD of V-NAND device wafer image by ISR. (b) One chip die enlarged figure and (c) decapsulation microscopic inspection results.

increase, especially at the point where the ISR BCD is less than 91.4%, where CHH NOPs are clustered. This shows that although ISR is a non-destructive technique that measures the mold region undamaged, it can achieve results comparable to optical microscopy after sample destruction.

The result demonstrates the advantages of hyperspectral imaging technology. The ISR image has a resolution that is limited by the pixel size of the two-dimensional CMOS without an objective lens to further increase the resolution. Therefore, a monochromatic ISR image cannot provide a distribution for a CHH diameter of several nanometers. However, continuous-wavelength images are combined to obtain spectroscopic information from each pixel, and by analyzing them with deep learning models, the size of the nanometer structural group can be obtained. In other words, insufficient resolution of optics can be overcome using spectroscopic information. Furthermore, the results confirm that it is possible to non-destructively determine the size of substructures in CHH, a HAR structure, by utilizing wavelength regions with high penetration depth such as near-infrared.

3.3 Detecting Chip Die with NOP Failure with ISR

After completing the verification of the small quantity as shown above, the metrology step for measuring the ISR after the etching process of forming CHH was set for the V-NAND product. Instead of measuring the entire die on the wafer, to minimize the measurement time during the evaluation, 36 dies were selected from the outermost dies as shown in Fig. 4(a). The 36 selected dies are categorized into three groups: those with mainly normal CHH formation, those with small CHH BCD but not up to NOPs, and those with mainly NOPs, as shown in Fig. 5 with gray dots (normal), blue triangles (low BCD), and red x (discarded), respectively. Among them, the area of dies with normal CHH and small CHH BCD but not up to NOPs are exposed normally in the photolithography process for the subsequent word line generation process, but the chip die areas with a large number of NOPs are prevented from being exposed and become discarded wafer areas. From the ISR measurement, there are numerous BCD values in a chip die as shown in Fig. 4(b). Among them, the minimum BCD value per chip was calculated and recorded as "ISR BCD MIN". In addition, a cross-measurement of conventional spot SE was performed during the same period for comparison. After the entire integration processes of the measured device wafer were completed, the metrology results were compared with the electrical die sorting analysis and their correlation was confirmed, as shown in Figs. 5(a)–5(d).

When checking the correlation between the failure rate related to CHH NOP and SE BCD, the boundary between discarded and normal chips cannot be distinguished as shown in Fig. 5(a). On the other hand, in the case of ISR BCD MIN, the discarded and normal chip can be distinguished by 88.6% of the target CD, as shown in Fig. 5(c). Therefore, it is possible to select the case where the CHH formation is as successful as the normal chip among the dies designated as unexposed for photolithography after the CHH etching process. As shown in Figs. 5(e) and 5(f), the CHH BCD of the chip die marked with the blue arrow is formed high, unlike other discarded near-edge dies, and the level of BCD is the same as the low BCD chips that are exposed for subsequent photolithography process. Therefore, based on the accumulated trend of the ISR, the die is sufficient to be converted into an exposure area in the subsequent photolithography process.

In the case of the result of excluding the discarded chip, the correlation between the BCD measured in the chip in which the normal CHH is formed, as shown in Figs. 5(b) and 5(d), and the defect rate can be confirmed. For the SE BCD, the correlation with the defect rate is low, $R^2 = 0.41$, while the ISR BCD MIN is high, $R^2 = 0.82$, which is twice that of SE. It means that ISR BCD MIN is more suitable for monitoring etching process equipment than SE BCD. Actually, the method of obtaining BCD from SE signal also uses a deep learning model in the same way as ISR in Samsung. In addition, SE inherently contains the phase information of light, which is more advantageous in accurately inferring the structure size than ISR, an SR signal with only the simple intensity of reflectivity. Furthermore, the BCD difference between SE and ISR for 1600 measurement points is 9.87%, which is less than 10%. Therefore, the difference in CHH defect detection capability between these two technologies comes from whether it "measures the whole chip" or "measures with a fixed local location." In the case of ISR, the entire chip die is measured at once, so if there is a part of the defective point in the chip, it will be detected as

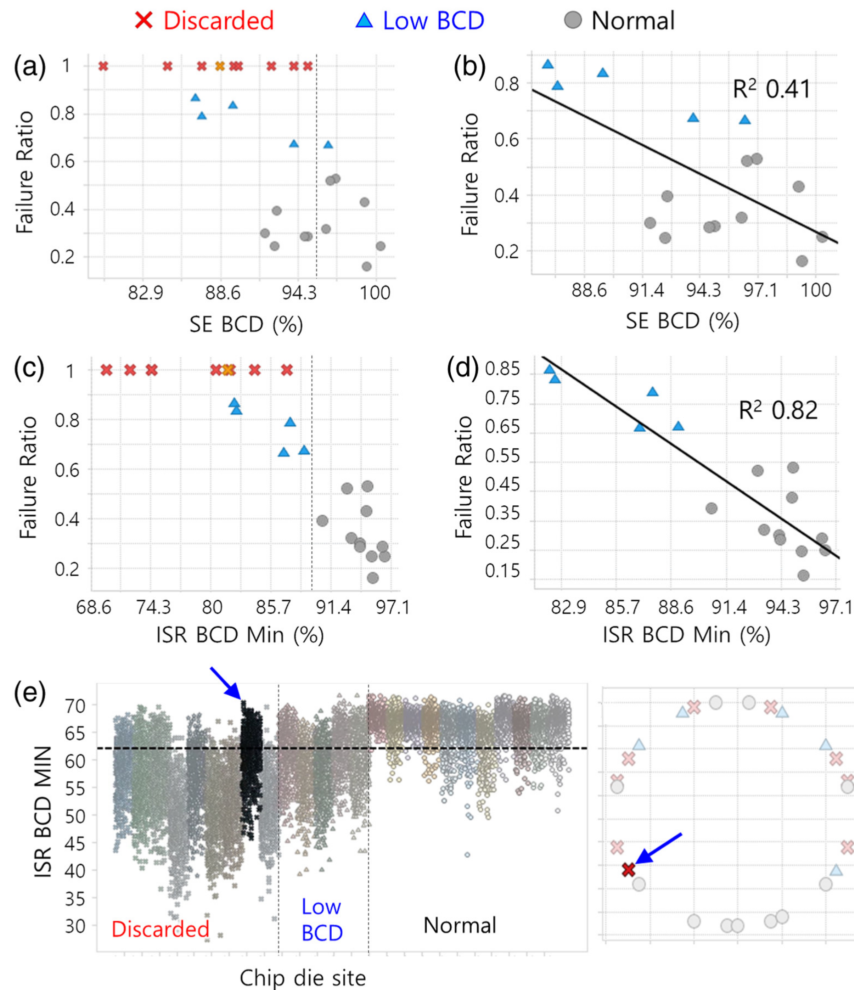

Fig. 5 (a)–(d) Correlation between CHH BCD of V-NAND product and CHH NOP-related defect rate measured after completion of device manufacturing. Red × corresponds to the outer chip that is not subsequently exposed, blue ▲ corresponds to the exposed outer chip, and gray • corresponds to the inner chip. Correlation between SE BCD and defect rate (a), (b), and correlation between ISR BCD MIN and defect rate (c), (d). (e), (f) Trend data of the ISR metrology step after the V-NAND CHH etching process for a certain period of time. The ISR BCD MIN trend of the chip indicated by the blue arrow (f) among the discarded chips is similar to that of the low BCD chips.

defective. On the other hand, in the case of conventional spot measurement technology, if there is no defect at the predetermined position in the chip die, the chip is judged to be normal. In particular, for area defects that appear on the chip at the wafer edge, it is difficult to select a single point that is representative of the entire chip because the starting location of the defect is variable within the die. To cover the area of a single ISR measurement with spot SE would require 44,000 measurements in this case, which is not realistically possible due to time constraints.

However, considering the large number of SE facilities already in operation on the production line, the comfort of engineers for familiar SE techniques, the period of adaptation to ISR until deep learning model construction, and the fast measurement speed compared to ISR, the overall mass productivity of spot SE facilities is superior to ISR. Therefore, it is necessary to use the spot SE facility until the mass production capacity of ISR is increased. Therefore, for now, the best way is to increase the number of sites measured in a single chip of spot SE by referring to the ISR results, then operate the measurement step by modifying the recipe by optimizing the site, and update the recipe or learning model by periodically cross-evaluating the ISR results.

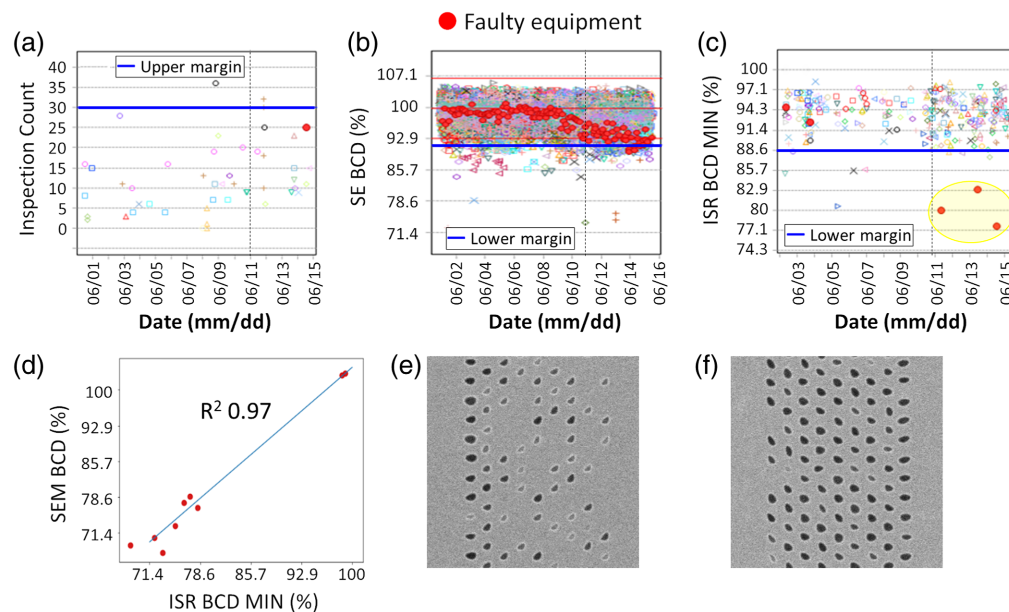

Fig. 6 Metrology trend data of (a) decapsulation inspection results, (b) spot SE, and (c) ISR for nine normal chips after the CHH etch process. (d), (e) Wafers etched with equipment identified as defective are marked with red dots. (d) Correlation between CHH BCD and ISR BCD MIN calculated from the decapsulation SEM image (e) for the wafer measured on June 13 among the wafers marked with red dots in Fig. 6(c). (f) Decapsulation SEM image of a normal case with no clustering of CHH NOPs.

3.4 Detecting Etch Equipment Failures Using ISR

After a high correlation between ISR and chip defect rate was confirmed, the number of measurement points in this metrology step was reduced to nine normal chips and utilized as anomaly detection monitoring for the etch facility. The inspection and metrology trends of decapsulation inspection, spot SE, and ISR were obtained after the etching process for CHH formation over a period of about 2 weeks. As shown in Fig. 6(c), the trend of ISR BCD MIN was found to be lower than the boundary value of 88.6% of target CD, indicated by the blue straight line, starting on June 12, for wafers processed in the etch facility, indicated by the red dot. On the other hand, during the same period, the trend of decapsulation inspection [Fig. 6(a)] and spot SE [Fig. 6(b)] showed that neither the NOP count nor the BCD of CHH etched by the problematic equipment was out of the boundary value and was determined to be normal. To determine which of the ISR and the other two techniques were detected correctly, a decapsulation SEM examination was performed on the wafers identified as defective CHH by ISR. The correlation between the BCD extracted from the decapsulation SEM image and ISR BCD MIN was found to be very high with $R^2 = 0.97$, confirming that ISR provided the correct measurement, as shown in Fig. 6(d). In addition, 14 out of 46 imaged areas in the decapsulation SEM were found to have a large amount of CHH NOPs as shown in Fig. 6(e). For reference, checking the images recorded for a normal chip die on 24 random wafers with decapsulation SEM measurements at a similar time, there were only four NOPs on average, as shown in Fig. 6(f). In other words, the wafers that were detected as anomalies in the ISR trend were determined to be poorly etched at the issuing facility.

In the previous case of Figs. 4(b) and 4(c), we observed that the decapsulation inspection and ISR images were obtained in a similar manner. However, in this case, the results were inconsistent. This inconsistency arises because, during the analysis of the optical image in the inspection process, it becomes difficult to identify defects when there is no hole formation in a large area. As a result, the decapsulation inspection fails to accurately detect clustered NOPs. On the other hand, ISR works by projecting bundles of NOPs onto the spectrum, and it is expected that similar cases have been learned through deep learning. Therefore, ISR appears to be capable of detecting NOP bundles successfully. In the case of Spot SE's failure to detect anomalies, it is expected that the measurement positioning is improper, as explained before.

4 Conclusion

Based on hyperspectral imaging and supervised deep learning, ISR has shown that the BCD of a V-NAND CHH can be quickly and non-destructively imaged for the entire chip die. Furthermore, metrology trends from ISR have been obtained and found to be highly correlated with the defect rate caused by CHH BCD NOPs in actual V-NAND mass production. By utilizing the ISR, we can quickly identify the appropriate etch conditions at the wafer edge, which is expected to increase the yield of V-NAND by reducing the edge exclusion area. It is also expected to be directly utilized in the metrology step of monitoring the CHH etch process equipment or to guide the sampling location of the wafer for spot SE measurement. In the future, Samsung expects to develop ISR into a HAR structure defect detection technology for various memory products, including the capacitor hole of DRAM as well as V-NAND.

Disclosures

The authors declare no competing interests.

Code and Data Availability

Data sharing is not applicable to this article, as it is Samsung's company policy that process information is confidential and cannot be shared externally.

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